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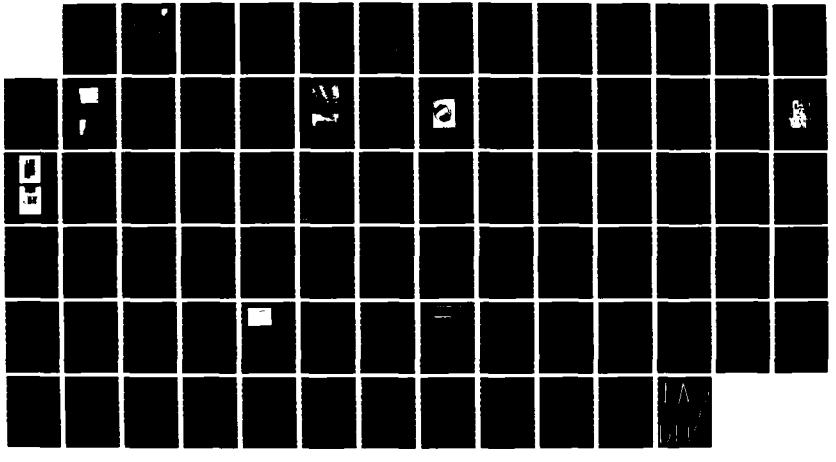

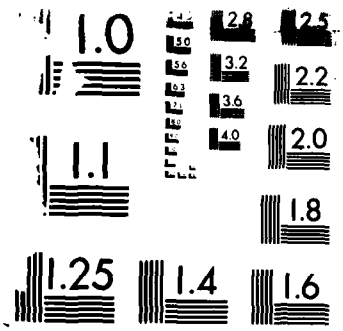

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RADC-TR-86-136
Interim Report
October 1986

# Si ON ALUMINA PHASE SHIFTERS

Rensselaer Polytechnic Institute

Edward W. Maby and Ronald J. Gutmann





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This effort was funded totally by the Laboratory Directors' Fund



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AD-A174 721

# REPORT DOCUMENTATION PAGE

| | |
|---|---|
| 1a REPORT SECURITY CLASSIFICATION<br>UNCLASSIFIED | 1b RESTRICTIVE MARKINGS<br>N/A |
| 2a SECURITY CLASSIFICATION AUTHORITY<br>N/A | 3 DISTRIBUTION / AVAILABILITY OF REPORT<br>Approved for public release; distribution unlimited |
| 2b DECLASSIFICATION / DOWNGRADING SCHEDULE<br>N/A | |
| 4 PERFORMING ORGANIZATION REPORT NUMBER(S)<br>N/A | 5 MONITORING ORGANIZATION REPORT NUMBER(S)<br>RADC-TR-86-136 |
| 6a NAME OF PERFORMING ORGANIZATION<br>Rensselaer Polytechnic Institute<br>6b OFFICE SYMBOL (If applicable) | 7a NAME OF MONITORING ORGANIZATION<br>Rome Air Development Center (ESM) |
| 6c ADDRESS (City, State, and ZIP Code)<br>110 8th Street<br>Troy NY 12181 | 7b ADDRESS (City, State, and ZIP Code)<br>Hanscom AFB MA 01731-5000 |
| 8a NAME OF FUNDING / SPONSORING ORGANIZATION<br>Rome Air Development Center<br>8b OFFICE SYMBOL (If applicable)<br>ESM | 9 PROCUREMENT INSTRUMENT IDENTIFICATION NUMBER<br>F19628-85-K-0038 |
| 8c ADDRESS (City, State, and ZIP Code)<br>Hanscom AFB MA 01731-5000 | 10 SOURCE OF FUNDING NUMBERS<br>PROGRAM ELEMENT NO: 61101F; PROJECT NO: LDPF; TASK NO: 10; WORK UNIT ACCESSION NO: C5 |

11 TITLE (Include Security Classification)
Si ON ALUMINA PHASE SHIFTERS

12 PERSONAL AUTHOR(S)
Edward W. Maby, Ronald J. Gutmann

| 13a TYPE OF REPORT | 13b TIME COVERED | 14 DATE OF REPORT (Year, Month, Day) | 15 PAGE COUNT |
|---|---|---|---|
| Interim | FROM Mar 85 TO Mar 86 | October 1986 | 84 |

16 SUPPLEMENTARY NOTATION
This effort was funded totally by the Laboratory Directors' Fund

| 17 COSATI CODES | | | 18 SUBJECT TERMS (Continue on reverse if necessary and identify by block number) |
|---|---|---|---|
| FIELD | GROUP | SUB-GROUP | diode phase shifters<br>silicon on alumina<br>melt recrystallization |
| 20 | 02 | | |
| | | | |

19 ABSTRACT (Continue on reverse if necessary and identify by block number)

P-i-n diode phase shifters for operation below 10 GHz require a relatively small diode area in relation to the overall microstrip circuitry. Recrystallization of silicon islands deposited on alumina substrates is being explored as a means of providing the necessary diode material. Initial crystallization experiments with an electron beam have identified refinements needed to the system. A diode design study favors a lateral over a vertical p-i-n structure and suitable masks are in preparation. A method of evaluating minority carrier lifetime in thin silicon films on insulators has also been developed and will be used to evaluate recrystallized films.

| 20 DISTRIBUTION / AVAILABILITY OF ABSTRACT | 21 ABSTRACT SECURITY CLASSIFICATION | |
|---|---|---|
| ☐ UNCLASSIFIED/UNLIMITED ☒ SAME AS RPT ☐ DTIC USERS | UNCLASSIFIED | |
| 22a NAME OF RESPONSIBLE INDIVIDUAL<br>Dr. Daniel Eirug Davies | 22b TELEPHONE (Include Area Code)<br>(617) 377-3921 | 22c OFFICE SYMBOL<br>RADC (ESM) |

DD FORM 1473, 84 MAR — 83 APR edition may be used until exhausted. All other editions are obsolete.

SECURITY CLASSIFICATION OF THIS PAGE
UNCLASSIFIED

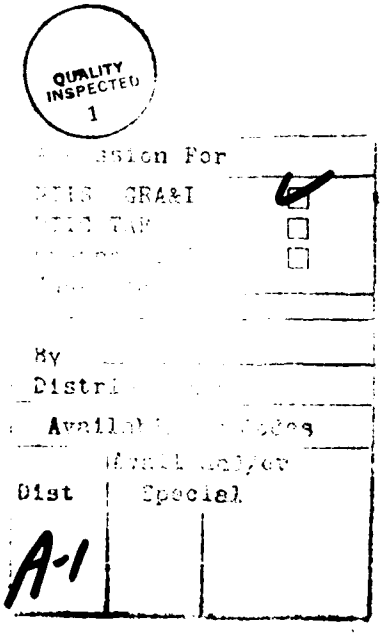
## ABSTRACT

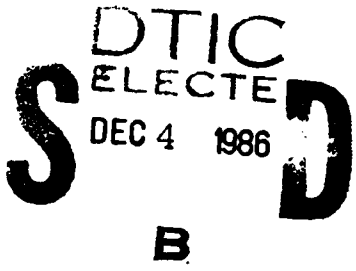
This research program is aimed toward a microwave monolithic integrated circuit (MMIC) technology using recrystallized silicon-on-insulator substrates. Such a technology would permit PIN diode phase shifters to be fabricated with higher power-handling capability and lower insertion loss than conventional MMIC control circuits using GaAs MESFETs. Moreover, at frequencies below 10 GHz, where substrate area requirements can be extensive, the silicon-on-insulator substrate technology can be less expensive. This research program stresses silicon-on-alumina recrystallized films, followed by growth of silicon epitaxial layers and surface-oriented PIN diode fabrication.

In the first year of the program we have accomplished the following:

1. initial recrystallization of sputtered silicon on alumina with a CVD $SiO_2$/sputtered $Si_3N_4$ encapsulation layer and an evaluation of recrystallization difficulties.
2. modification of an electron-beam system to permit controlled recrystallation experiments.
3. a design tradeoff of surface-oriented PIN diodes versus vertical devices for MMIC applications.
4. evaluation of microwave-detected photoconductivity decay as a measurement technique for thin-silicon-film recombination lifetime evaluation.
5. definition of a program plan for the second year.

The principal investigators acknowedge the capable assistance of Mr. T. Letavic in executing many of the tasks of this program and the encouragement and support of the contract monitor, Dr. Eurig Davies.



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## 1. INTRODUCTION

Monolithic microwave integrated circuits (MMICs) containing transceiver (transmitter/receiver) circuitry have not been incorporated into microwave systems principally because of either inferior performance and/or excessive cost. The high costs result from an expensive technology base (usually epitaxial GaAs channels on semi-insulating substrates or ion-implanted channels), inadequate use of wafer area (due to the large-area requirements of the passive circuitry) and the relatively small number of transceivers needed in microwave systems compared to digital applications (even with planar phased arrays). Si PIN diodes have significantly enhanced RF performance compared to GaAs MESFETs for control applications like phase shifting, since both switching figure-of-merit and power-handling capability are increased. However, production reproducibility, performance advantages due to lower parasitics and lower cost potential drive innovative research in MMICs for this, and other, microwave applications.

Most of the research in MMICs involves GaAs epitaxial layers (or in some cases ion-implanted layers) on semi-insulating GaAs. The technology suffers from yield problems, since large areas of device-quality layers are mandatory. In most technologies to date, GaAs metal-semiconductor (or Schottky-gate) field-effect transistors (MESFETs) are the active device building blocks. These versatile devices have been used not only in traditional transistor applications such as low-noise and power amplifiers, but also in frequency conversion (e.g. mixers) and control (e.g. switches and phase shifters) components. Performance as a control device is particularly poor compared to Si PIN diodes because of the relatively large on-resistance (~ 4 to 10 ohms) inherent with the device structure and the

limited RF voltage capability (~ 20 to 30 volts drain-to-source). The high resistance results in appreciable dissipation in the device and reduced average-power handling capability, while the reduced voltage handling results in low peak-power performance. Recent results indicate that GaAs PIN diodes may become viable control devices, with applications in MMIC technology. However, the relatively low lifetime (~ 10 to 100 nanoseconds for lightly-doped high-quality GaAs) of this direct-band-gap material forces thin I-layer dimensions and relatively low peak-power capability compared to Si PINs.

While GaAs MMICs are being established as a viable technology, the production cost of such a technology remains a serious concern. In this program, silicon-on-insulator (SOI) technology is investigated as a potential alternative offering the promise of lower cost as well as improved control-component performance. Conceptually, a silicon film is deposited over a microwave-quality dielectric substrate and recrystallized, serving as a base for further processing. Such a silicon-on-insulator technique would result in a monolithic microwave technology which is:

1) compatible with highest control-device figure-of-merit and highest control-device power handling, namely the Si PIN diode
2) potentially a much lower cost technology than GaAs MMICs
3) compatible with high-power system requirements below 10 GHz
4) potentially extendable to other semiconductors (including compound semiconductors), perhaps on the same substrate.

The two-year research program is concerned with the initial evaluation of the feasibility of a silicon-on-insulator MMIC technology. In particular, the program has focused on PIN diodes for a 40-watt, 5.3-GHz, low-loss monolithic phase shifter as a test vehicle. While fabrication of a

complete phase shifter is beyond the scope of the research, we hope to delineate key problems affecting the technology and evaluate the potential for future microwave systems. PIN diodes are particularly difficult for a silicon-on-insulator technology since a reasonable high-injection-level recombination lifetime is needed to obtain conductivity modulation under forward bias. However, they are critically important in transceiver modules for phased arrays and therefore an excellent test vehicle for evaluating the potential of a silicon-on-insulator technology for MMICs.

At present, a monolithic 40-watt peak power, 4-watt average power, 5.3-GHz, low-loss phase shifter cannot be realized in either GaAs or Si. In GaAs, the large on-resistance of MESFETs results in high loss and low average-power handling capability. In addition, the peak-power handling capability is limited by drain-to-source breakdown to less than 10 watts. GaAs PINs have minority carrier lifetimes which are too low and, therefore, thin I layers and low peak-power handling capability. While the phase-shifter requirements are well within the capability of Si PIN diodes, the lack of semi-insulating silicon substrates with sufficient dielectric quality is incompatible with conventional semiconductor monolithic implementation. More specifically, the dielectric loss of a silicon MMIC transmission line prohibits high-performance circuits.

The actual PIN diode requirements depend not only on the phase-shifter component specifications (5.3 GHz, 40 watts peak, 4 watts average, 0.5 microseconds switching time) but also on the phase-shifter circuit design. However, the PIN diode/phase shifter circuit designs are mutually coupled by the material/device performance capabilities. To guide the material/device research program for a silicon-on-insulator technology, we conservatively assume that the PIN diode must handle twice the RF line voltage under

reverse bias and twice the RF line current under forward bias. That is, we assume that the PIN diode is capable of performing as a single-pole-single throw switch. Assuming a 50-ohm transmission line and conservative silicon PIN diode design rules, we arrived at a 3-mil-diameter diode with 12-μm I-layer thickness for a conventional vertical diode configuration. Additional aspects of the PIN diode design, a comparison of lateral and vertical configurations and our best estimate of performance capability is discussed in Section 4.

A suitable substrate for MMIC applications must have a low-loss tangent dielectric with large thermal conductivity and a coefficient of expansion closely matched to silicon, and it must be available at reasonable cost. The silicon film over the substrate must be free from macroscopic defects and possess long carrier lifetime. Both cost and lifetime factors preclude the choice of silicon-on-sapphire, the only thin-film SOI system which can be produced by heteroepitaxial growth. To date, most other SOI technologies have produced thin silicon films over an oxidized silicon substrate by means of a solid- or liquid-phase recrystallization process. However, for the MMIC application, the underlying silicon layer would provide undesired dielectric loss and negate the advantage of recrystallized film processing.

A substrate which meets many MMIC requirements is alumina, as it is already used as a substrate in hybrid MICs and, in single-crystal form (i.e., sapphire), as a substrate for silicon field-effect devices. Recent work has shown that polycrystalline silicon films can be recrystallized over a sapphire substrate by a liquid-phase process, and the electrical characteristics of these films are similar to those for conventional heteroepitaxial silicon-on-sapphire. A similar recrystallization process for polycrystalline silicon deposited over alumina should produce improved

results since the thermal expansion of alumina can be better matched to that of silicon.

Thus, this research program emphasizes recrystallization of silicon-on-alumina, with evaluation of the suitability of these films for subsequent PIN diode fabrication and MMIC implementation. The remainder of the report covers:

- o silicon-on-alumina recrystallization concepts, test structures and initial results
- o electron-beam system design and performance characteristics
- o PIN diode device alternatives and mask design
- o recrystallized film characterization, including a novel technique for lifetime measurement
- o plans for the second year of the program.

## 2. SILICON-ON-ALUMINA RECRYSTALLIZATION

In this section, we present an overview of recrystallization research which serves as a foundation for our technical approach (Section 2.1), followed by a discussion of the factors important in sample preparation prior to the actual recrystallization process (Section 2.2). Finally we present our initial results to date, along with our evaluation of the initial recrystallization experiments (Section 2.3).

### 2.1 Technical Background

Liquid-phase processes for the realization of single-crystal silicon films over various insulating substrates all require the movement of a molten silicon zone over the substrate surface. The processes differ mainly by the shape of the molten zone and the type of heat source which is used.

First experiments used a focused laser beam to produce a molten spot with circular symmetry,[1] and later recrystallization results were improved by judiciously shaping the spot.[2] Other experiments have used a resistively-heated graphite strip[3,4] or an electron beam[5,6] to produce a molten line.

Apart from the results of various crystallographic diagnostic procedures, one measure of the success of a recrystallization experiment is the channel carrier mobility and sub-threshold leakage current of insulated-gate field-effect transistors fabricated on the recrystallized film. For the case of oxidized silicon substrates, line-source experiments have produced the best, and most consistent, device results thus far.[3,7,8]

Typical recrystallization results for the case of 0.5-μm-thick silicon films and a graphite-strip source are shown in Fig. 2.1. As indicated by the orientation pattern of a matrix of anisotropically etched square pits (pit grid), the recrystallized silicon films consist of large (2 mm x 1 cm) grains which are seeded from a transition region at the edge of the film and separated by large-angle grain boundaries. Within the large grains, at approximate 25-μm intervals, are line defects which are generally parallel to one another and to the scan direction of the graphite strip. These parallel line defects are surface intersections of planar defects that cut the entire film thickness more or less perpendicularly; they are believed to be associated with angular deviations of the order of one degree or less, so they are called subboundaries.[4] The films have nearly uniform (100) crystallographic texture.

Experiments have shown that majority-carrier transport is impeded by large-angle grain boundaries which transversely cross resistor bars fabricated in recrystallized silicon films, and the turn-on characteristics of similarly oriented field-effect transistors are also influenced.[9]

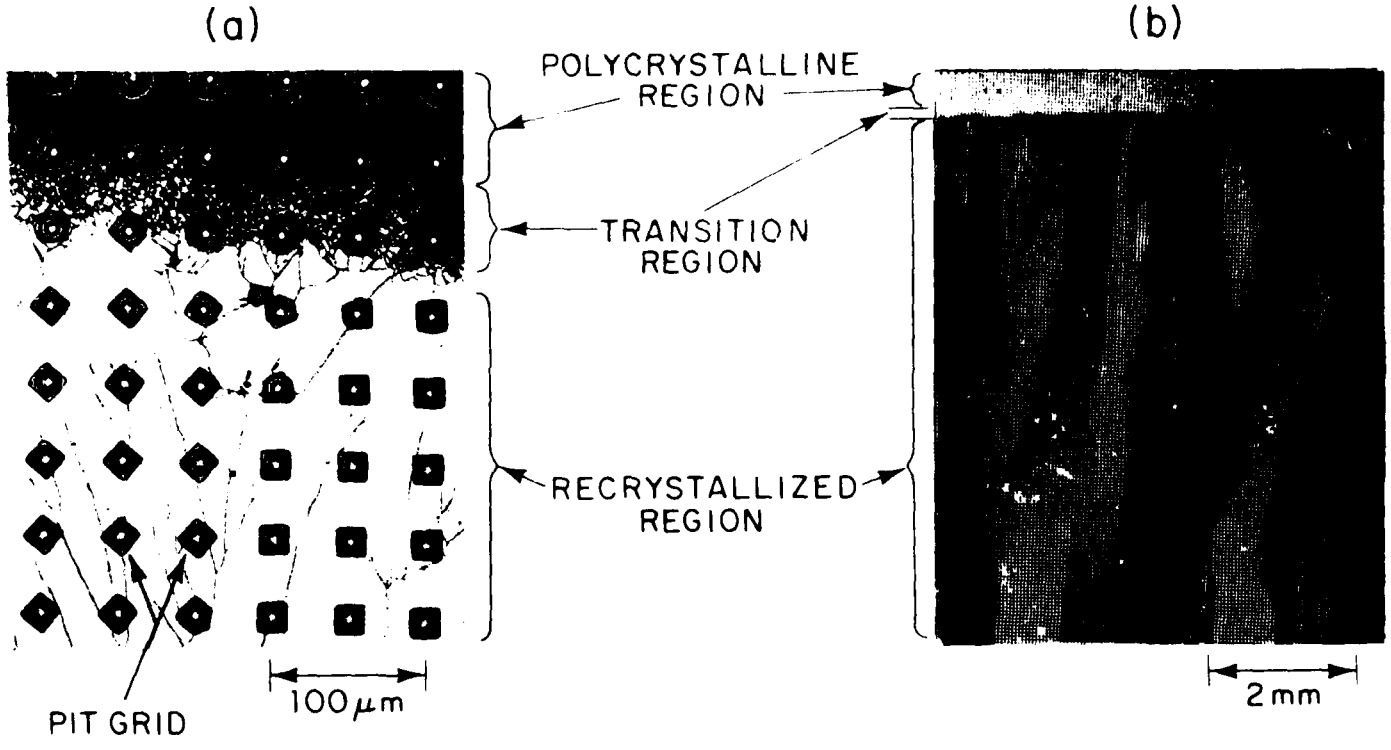



Fig. 2.1 Typical line-source recrystallized films (see text).

Enchanced diffusion of impurities along large-angle grain boundaries can also merge the source and drain regions of parallel-oriented field-effect transistors.[10] Fortunately, the density of large-angle grain boundaries can be reduced by double-pass recrystallization or substrate seeding.[11] Subboundaries have relatively little influence on majority-carrier bulk transport or the turn-on characteristics of field-effect transistors, and the degree of lateral diffusion along subboundaries is much less than that for large-angle grain boundaries. Subboundaries must be avoided, however, when minority-carrier lifetime is important.[12] Although it is not possible to completely eliminate subboundaries from thin line-source-recrystallized films, special procedures can be employed to confine the subboundaries to specific positions so that devices can be fabricated in between them.[13]

There have been a limited number of line-source recrystallization experiments which concern silicon over sapphire and fused quartz.[14,15] For the case of sapphire substrates, the recrystallized silicon film is under compressive stress; whereas, for the case of fused-quartz substrates, the recrystallized silicon film is under tensile stress, and care must be taken to avoid the formation of cracks in the film.

The silicon-on-sapphire line-source recrystallization results suggest that high-quality silicon-on-alumina films for the fabrication of PIN diodes can be produced by a similar procedure. For our experimental program, we have chosen to use a rapidly scanned electron beam in order to approximate a line source since we believe that this is superior to a graphite-strip or an arc-lamp source in terms of control of the molten zone. The electron-beam system has required considerable development (see Section 3), so we have employed a graphite-strip recrystallization apparatus from time to time during the course of our program.

## 2.2 Factors Influencing Sample Preparation

Line-source recrystallization experiments have all employed some form of encapsulation layer over the silicon film in order to induce recrystallized film texture and promote wetting of the substrate beneath the film. For the case of oxidized silicon substrates, the film texture is made more uniform as the thickness of a chemical-vapor-deposited (CVD) silicon dioxide encapsulation layer is increased,[16] but the improvement is marginal for thicknesses greater than about 2 μm. Studies have shown that the agglomeration problem tends to be avoided if nitrogen is present at the interface between the silicon film and the encapsulation layer prior to recrystallization.[17] This has been achieved by sputtering silicon nitride over the silicon dioxide encapsulation layer[3] and by depositing the silicon dioxide with a plasma CVD process which uses $N_2O$ as a source gas.[18] The specifics of encapsulation-layer preparation remain less of a science than an art.

The stresses on the encapsulation layer are reduced as the width of the molten zone is decreased. We expect that the electron-beam line source will yield a more narrow molten zone than that which is produced by a graphite strip or arc lamp, so the electron-beam recrystallization experiments may be relatively forgiving in terms of the agglomeration problem.

By tradition, most silicon-on-insulator recrystallization experiments have used 0.5-μm-thick silicon films. Thicker films lead to increased subboundary spacing,[16] and significant reduction in defect density is observed in thick films when the encapsulation layer is patterned to provide vent openings for excess oxygen which is dissolved in the molten silicon.[19]

## 2.3 Recrystallization Results

Recrystallization experiments have been divided into two categories: those which concern silicon-on-insulator recrystallization in general (for the development of the electron-beam apparatus) and those which concern silicon-on-alumina recrystallization specifically (for the development of this material).

The former set of experiments have used the same sample characteristics as in other experiments.[3,4] The samples consisted of 0.5-μm-thick LPCVD polycrystalline silicon films over oxidized silicon substrates. The encapsulation layer consisted of a 2.0-μm-thick CVD silicon dioxide film and a 300-A-thick sputtered silicon nitride film.

The first electron-beam recrystallization results with these samples are shown in Fig. 2.2. The encapsulation films have been removed. Fig. 2.2a shows the film characteristics which result if the electron-beam current is too large. The chevron patterns are portions of the silicon film which have agglomerated, and the lower silicon dioxide layer appears to be damaged. Fig. 2.2b shows the results when the beam-current density is reduced. The top portion of the photograph shows unrecrystallized polycrystalline silicon. Below this is a dark band of large-grain polycrystalline silicon which has seeded the recrystallized film at the bottom of the photograph. The tree-like lines in the recrystallized film are subboundaries which have been decorated by a slow-acting silicon etch.

The electron-beam recrystallization results suggested the feasibility of the system, but many improvements were necessary. These system modifications are discussed in Section 3.

For a first set of silicon-on-alumina recrystallization experiments, 2-inch-square hybrid-grade alumina substrates were purchased from the

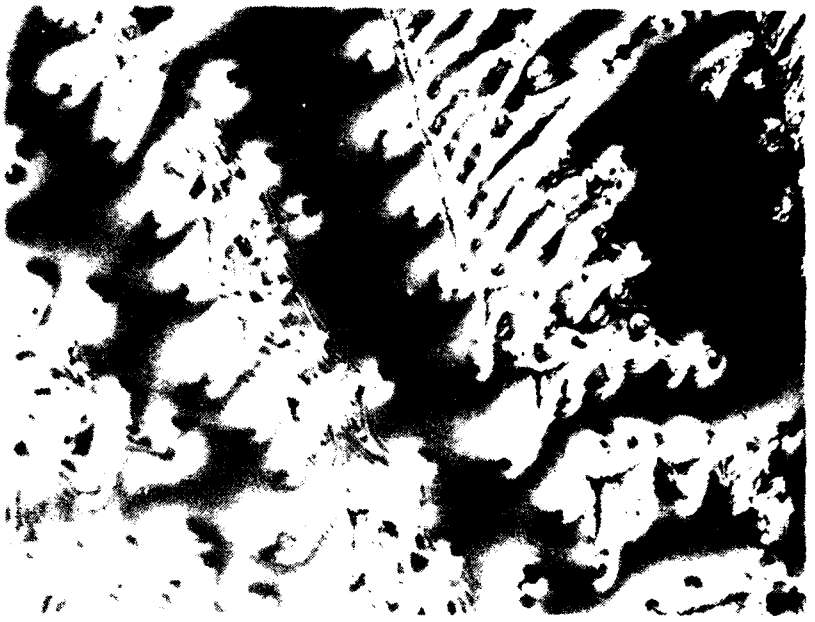


Fig. 2.2a Agglomeration of silicon thin film. The chevron patterns are agglomerated silicon and the wavy patterns are the damaged interface oxide.

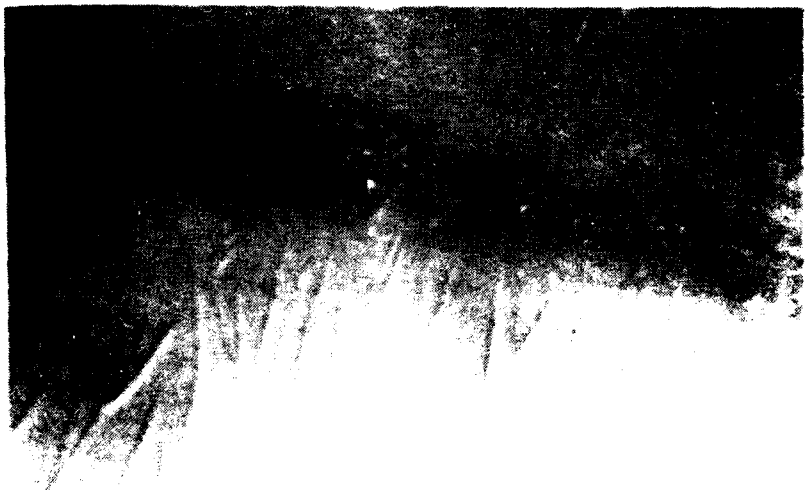


Fig. 2.2b Recrystallized silicon. The branching structures are subgrain boundaries which were decorated with a crystallographic etch.

Materials Research Corporation. The minimum surface-roughness specification which could be obtained was +/- 0.1 μm. A silicon film with 0.5-μm thickness was sputter deposited over the alumina; thicker films will be considered in future experiments. The encapsulation layer consisted of a 400-A-thick silicon dioxide layer sputtered in a nitrogen-rich ambient (so that nitrogen would be present at the interface between the encapsulation layer and the silicon), a 2.0-μm-thick CVD silicon dioxide layer and a 300-A-thick sputtered silicon nitride layer. This work was performed by Spire, and it represents their best approximation to the encapsulation films used for recrystallization experiments at other laboratories.

In order to test the samples for agglomeration resistance, first recrystallization experiments were performed with a graphite strip heater rather than waiting for completion of the electron-beam system modifications. The results were not successful. As shown in Fig. 2-3, the encapsulation layer suffered severe blistering from the silicon film beneath it. We believe that this is due to excess nitrogen which is trapped beneath the encapsulation layer, so the procedure for producing the encapsulation layer must be modified. The alternative sample preparation procedures which are currently under consideration are discussed in Section 6.

## 3. ELECTRON-BEAM SYSTEM CHARACTERISTICS

The electron-beam apparatus in operation at Rensselaer was designed with the intent of evaluating the feasibility of beam recrystallization of various materials including silicon-on-alumina. The test results of the initial SOI experiments were analyzed, and subsystem performance was evaluated. The redesign of several subsystems of the electron-beam system

Fig. 2.3 SEM photograph of the silicon-on-alumina encapsulation film after blistering.

became necessary in order to provide the largest possible process latitude. This section contains a synopsis of all the electron-beam system modifications, and current system performance capabilities are outlined.

## 3.1 System Redesign for SOI Research

In SOI experimentation, it is desirable to provide a substrate heating bias to elevate the sample temperature to 1000-1100°C prior to application of the scanned electron beam. The substrate temperature bias serves to reduce thermal gradients in the sample and to reduce the total beam power necessary to recrystallize the material. During the feasibility studies, it was observed that the arc lamp heaters used to provide substrate temperature bias operated under a temporal limitation; the arc lamps would extinquish after a few minutes of operation. It was discerned that heat transfer problems limited the operation of the arc lamps, and a new arc lamp assembly was designed and fabricated that would provide water cooling to the reflective mirror and to the mechanical supports for the arc lamps. The mechanical supports were machined out of stainless steel and bored out to create a water jacket. It is advantageous to use the same external water cooling lines for the reflective mirror jacket and the mechanical support jacket. One of the mechanical supports rests at the same potential above ground as the arc lamps, so the mechanical supports must be electrically isolated from the reflective jacket. Isolation was achieved by insertion of Ceramaseal water vacuum breaks. The entire assembly is grounded to chassis ground (except the mechanical supports) to reduce beam charging affects.

To discern the feasibility of SOI materials in an MMIC format, very large areas must be recrystallized so integrated circuits may be fabricated.

The large-area requirement indicates that the scan length of the electron-beam raster scan must be as large as possible. To maximize the scan length, the separation between the target plane and the deflection plates must be maximized, and the potential difference between the deflection plates must be maximized. The original electron-beam system was designed for small-area recrystallization only, so these design changes were carried out. The separation distance between the target plane and the deflection plates was increased by insertion of two one-inch vacuum flange spacers between the deflection plates and the target plane. The original column geometrical length was designed to yield a beam of minimum waist at the target plane. The insertion of the spacers results in a change in column optics, but this change is compensated by an adjustment of the variable anode position within the electron gun assembly. Thus, the increase of the column length has little or no effect on column optics.

A focusing magnet is mounted above the deflection plates. It is sometimes advantageous to intentionally defocus the beam, as with experiments designed to investigate the stability of the zone melt front. The stability of the zone melt front is a function of melt width (hence, beam diameter) and the translation rate of the molten zone..

It is evident that in order to maximize the raster scan distance, the potential difference between the deflection plates must also be maximized. However, when the electron beam is deflected close to a deflection plate, a significant amount of charge is induced on the plate, and the beam power is reduced at the target plane. A compromise between raster scan distance and target power requires a maximum deflection voltage of 2 KV. The scanning amplifier which produces the 2-KV output for deflection must also possess sufficient bandwidth so that the electron beam can approximate an ideal line

source. Recent published results indicate that a raster-scan frequency of 100 kHz is sufficient to maintain a constant thermal profile along the recrystallization front. The original vacuum-tube circuitry for the scanning amplifier was upgraded utilizing a two-stage amplifier configuration. Sharp-cutoff pentode receiving tubes were utilized in the low-voltage first stage of the amplifier and beam-power tubes were utilized in the high-voltage second stage of the amplifier. The input to the first stage of the amplifier consists of a DC offset and an AC deflection waveform with frequency between 40 kHz and 200 kHz.

The translation rate of the molten zone is an important factor in any recrystallization experiment. A new translation table was required in order to achieve better control over this experimental parameter. The translation table is mounted directly on top of the substrate heating assembly. It must sustain high temperatures for long periods of time, so the translation table was fabricated from quartz and machineable ceramic (Macor). The table drive system consists of a double-threaded shaft drive mounted on each side of the arc-lamp heating assembly. A double stainless-steel bolt drive was utilized to minimize the binding of the translation table due to uneven friction with the arc lamp housing. The drive system for the translation table consists of a gear and chain assembly. High-quality gears are mounted on each of the threaded stainless-steel drive shafts, and a stainless-steel chain slaves both drive shafts to a rotary-motion feedthrough in the electron beam chamber. The rotary motion feedthrough is driven by a variable-speed electric motor.

The translation table is also equipped with a molybdenum plate as a dead zone when initializing the electron beam. The surface of the molybdenum plate is in the same plane as the sample to facilitate focus

adjustments, and it serves as a remote beam-current sensing element. The translation table also contains a R-type thermocouple port for remote sensing of the sample temperature.

The subsystem improvements have been completed. The improved electron-beam system can be used to investigate the most important parameters of zone-melt recrystallization of SOI materials. The variable beam-current supply, variable raster-scan rate, and variable substrate-temperature bias provide the means for definition of a power window for optimum recrystallization results. The focusing-defocusing mechanism and variable translation speed provide the ability to quantify the stability of the recrystallization front. Experimentation during the second year of the program will help to better define these processing parameters.

### 3.2 Electron Beam System Capabilities

This section provides a synopsis of the electron-beam system capabilities due to the improved subsystem designs outlined in the preceding section. The capabilities are presented in terms of beam characteristics and subsystem performance data.

The electron-gun assembly offers the choice of two different filament types, one for low-power and one for high-power operation. The low-power filament produces up to 7 ma of beam current, while the high-power filament can deliver up to 30 ma of beam current. The minimum beam diameter on target is 85 μm, and the beam can be continuously defocussed up to 500 μm diameter. The beam deflection circuitry operates at 100kHz with an output voltage of 1800 V pp. The resulting scan length on target is 1.8 cm. The

scanning circuitry is capable of operating in a range from 40 kHz to 200 kHz.

The substrate heating assembly provides a substrate temperature bias from 300°C to 1100°C. The subsystem maintains vacuum integrity down to 3 x $10^{-7}$ torr, the base pressure of the system. The mechanical arc lamp supports are isolated from the lamp housing by 5kV water breaks. Beam-charging effects or glow-discharge phenomenon have not been observed.

The translation stage which controls the speed at which the molten zone traverses the sample has a nominal operating range of 0.05 to 4 mm/sec; thus, the system has high throughput capability. The translation table also provides beam positioning to within 10 μm. Vibrational pick up of the translation stage while it is moving is minimal, and no binding during translation has been observed.

## 4. PIN DIODE DESIGN

In parallel with our dominant emphasis on initial silicon-on-alumina recrystallization experiments and redesign and characterization of our electron-beam system, a systematic design of PIN diodes for phase shifters was undertaken. To properly consider PIN diode design in the recrystallized silicon film, we initially present a complete review of the key aspects of conventional PIN design and then include the effects of starting with a recrystallized semiconductor film. Finally, mask designs for the alternative device topologies, vertical and lateral, are presented.

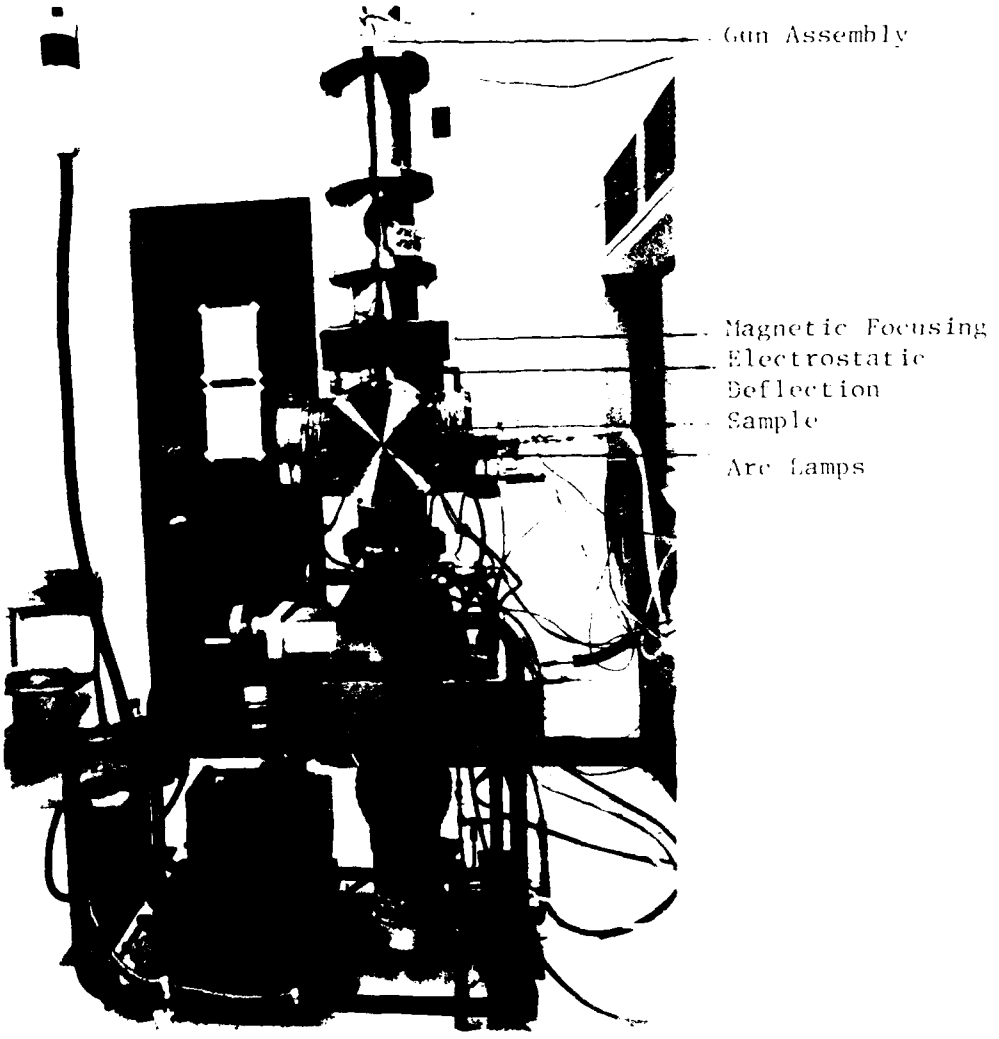
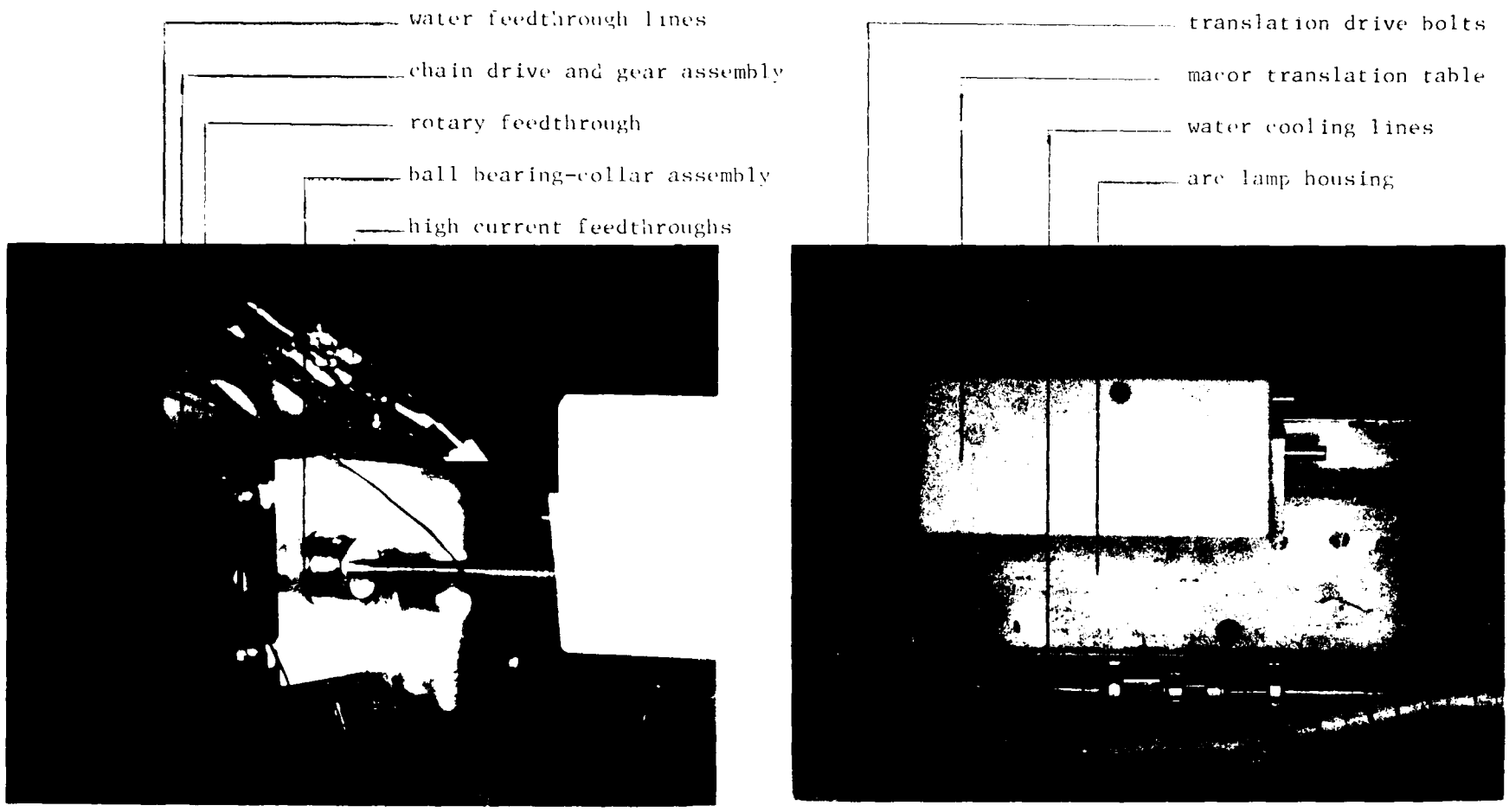



Figure 3.1 Photograph of Electron Beam Recrystallization Facility




45° with respect to viewport flange

90° with respect to viewport flange

Figure 3.2 Photographs from Viewpoint Into Electron Beam Chamber

## 4.1 Conventional PIN Diode

As presented in Appendix A, the key aspects of a PIN diode for microwave control applications are the following:

- o high-resistivity I layer for punch-through at low DC bias voltage (for low off-state loss)
- o high lifetime so that appreciable conductivity modulation can be achieved (for low on-state loss)
- o low parasitic resistances and capacitances so that inherent device capabilities are not degraded
- o uniform device structrure so that on-state injection is uniform and off-state premature avalanche does not occur.

This section presents the necessary relationships for the design of PπN diodes which should meet certain specifications for microwave switching applications. The most important operating parameters are the reverse bias capacitance, the reverse breakdown voltage, and the RF forward resistance. The diode design parameters are the resistivity $\rho_\pi$, the thickness W of the π region, the cross-sectional area A, and the depth of the diffused regions. The design relationships should allow the determination of the diode design parameters from the diode operating parameters.

The physical structure of a conventional vertical diode is shown in Fig. 4.1. In the planar structure depicted, the N region is a circular area of diameter d with an extended P region. For simplicity in the analysis, the above structure is idealized by assuming that the diode has a uniform cross-sectional area A, equal to the area of the N circle, and a π region of thickness W. This assumption is valid if W is small compared to d. The idealized structure is shown in Fig. 4.2.

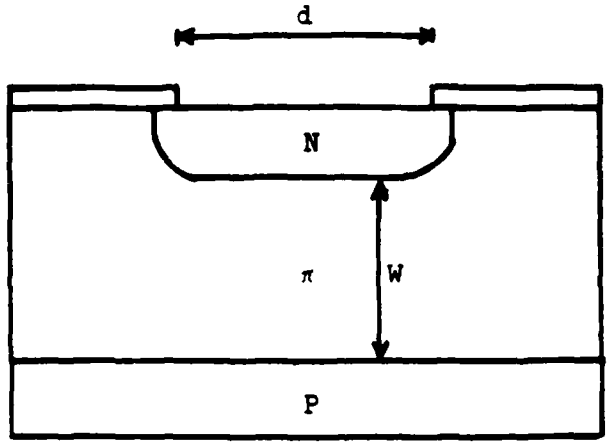



Fig. 4.1 Physical structure of a planar PπN diode

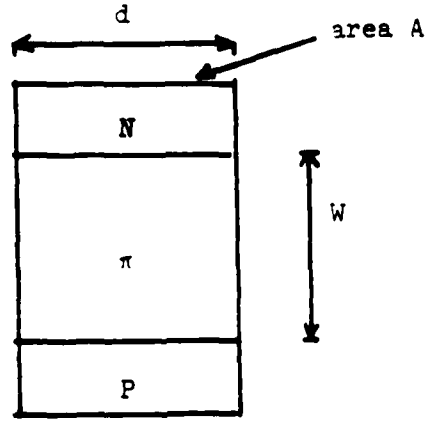



Fig. 4.2 Idealized structure of a PπN diode

The materials parameters which appear in the expressions for the operating parameters of a PπN diode are the electric permittivity, the mobility and diffusivity of electrons and holes, and the excess carrier lifetime. The key process-controlled parameter is the excess carrier lifetime, and this depends upon the type of recombination centers introduced during the fabrication processes.

The punch-through voltage, $V_p$, is the voltage required to deplete the π region. It can be calculated from Poisson's equation

$$V_p = \frac{q\, N_\pi\, W^2}{2\varepsilon} \quad , \tag{4.1}$$

or in terms of the resistivity of the π region, $\rho_\pi$:

$$V_p = \frac{W^2}{2\varepsilon \rho_\pi \mu_h} \quad , \tag{4.2}$$

where $\mu_h$ is the hole mobility. Equation (4.3) is plotted in Fig. 4.3 for the case of π-silicon. It is important to notice that the punch-through voltage is independent of the area of the device and that the same curve can be used to determine the voltage necessary for creating a depletion layer of thickness W in π-type material.

The capacitance of a depletion layer of cross-sectional area A and thickness W is a function of the applied reverse voltage, namely

$$C = A\left(\frac{\rho_\pi \varepsilon}{2\ \mu_h}\right)^{1/2} V_r^{-1/2} \tag{4.3}$$

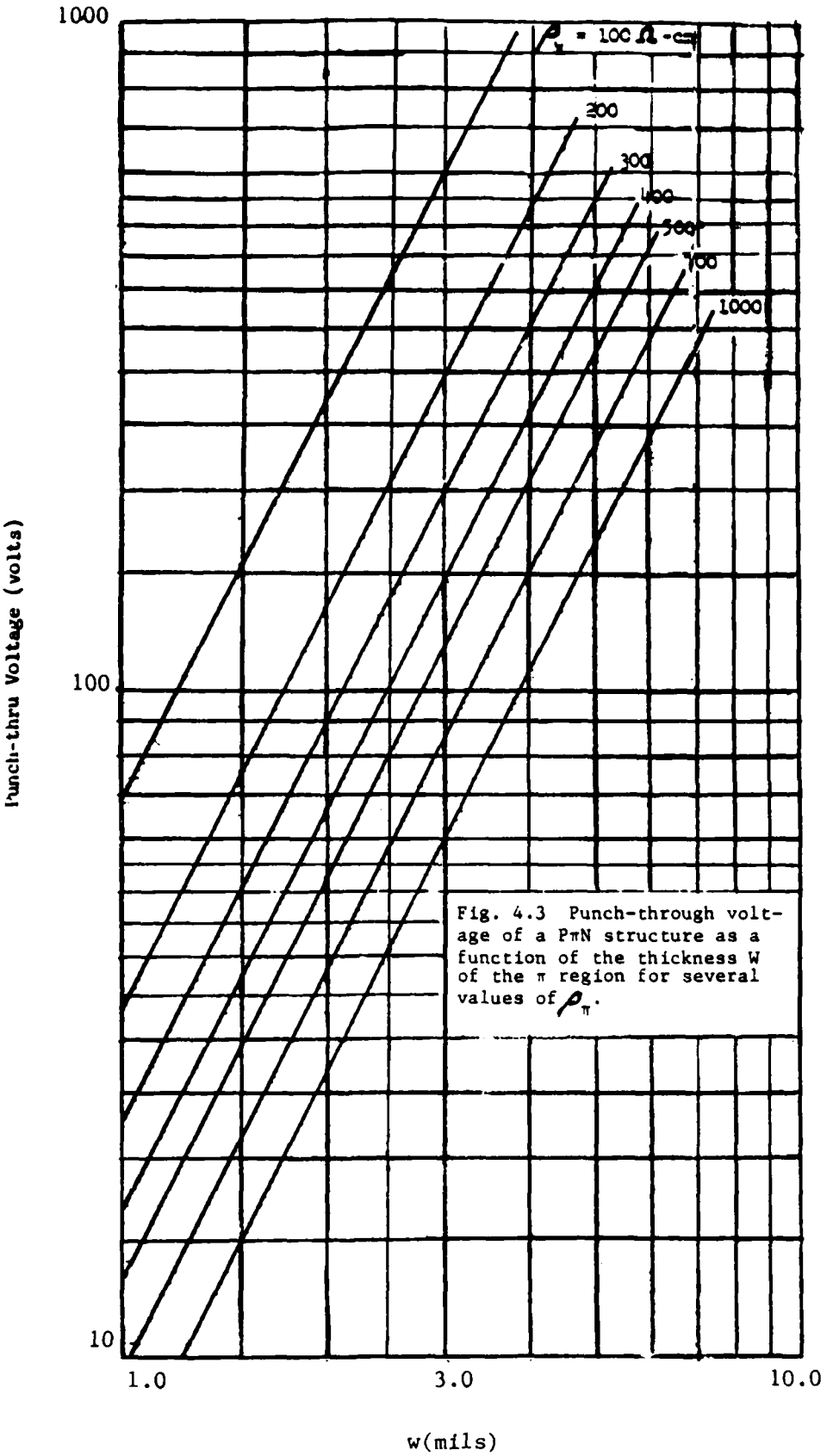



Fig. 4.3 Punch-through voltage of a PπN structure as a function of the thickness W of the π region for several values of $\rho_\pi$.

up to punch-through. After punch-through, the capacitance is constant and has the minimum value which can be achieved. The plot of Eq. (4.3) is given in Fig. 4.4 for the case of silicon.

If a reverse bias voltage $V_r (V_r \geq V_p)$ is applied to the PπN diode, the maximum electric field $E_m$ occurs at the Nπ junction and is given by:

$$E_{max} = \left( \frac{V_r - V_p}{W} \right) + \left( \frac{2V_p}{W} \right) = \frac{V_r}{W} + \frac{V_p}{W} \quad . \tag{4.4}$$

Avalanche breakdown occurs (approximately) when the maximum electric field reaches a critical value $E_{crit}$. The breakdown voltage $V_b$, obtained from Eq. (4.4), is given by:

$$V_b = W E_{crit} - V_p \tag{4.5}$$

If $V_p << W E_{crit}$ then:

$$V_b = W E_{crit} \tag{4.6}$$

The value of $E_{crit}$ depends upon the resistivity of the material. For material with bulk concentration less than or equal to $10^{14}$ carriers/cm$^3$, the value of $E_{crit}$ is $2 \times 10^5$ volts/cm or 500 volts/mil. Equations (4.5) and (4.6) are plotted in Fig. 4.5 using this value for the critical electric field and $\rho_\pi$ = 300 ohm-cm.

Equations (4.5) and (4.6) are valid for the case of a planar junction. In a planar fabrication process, the junction cross-sectional geometry is approximately cylindrical near the mask-defined junction edges, and the field distribution in the cylindrical part is different from that in the

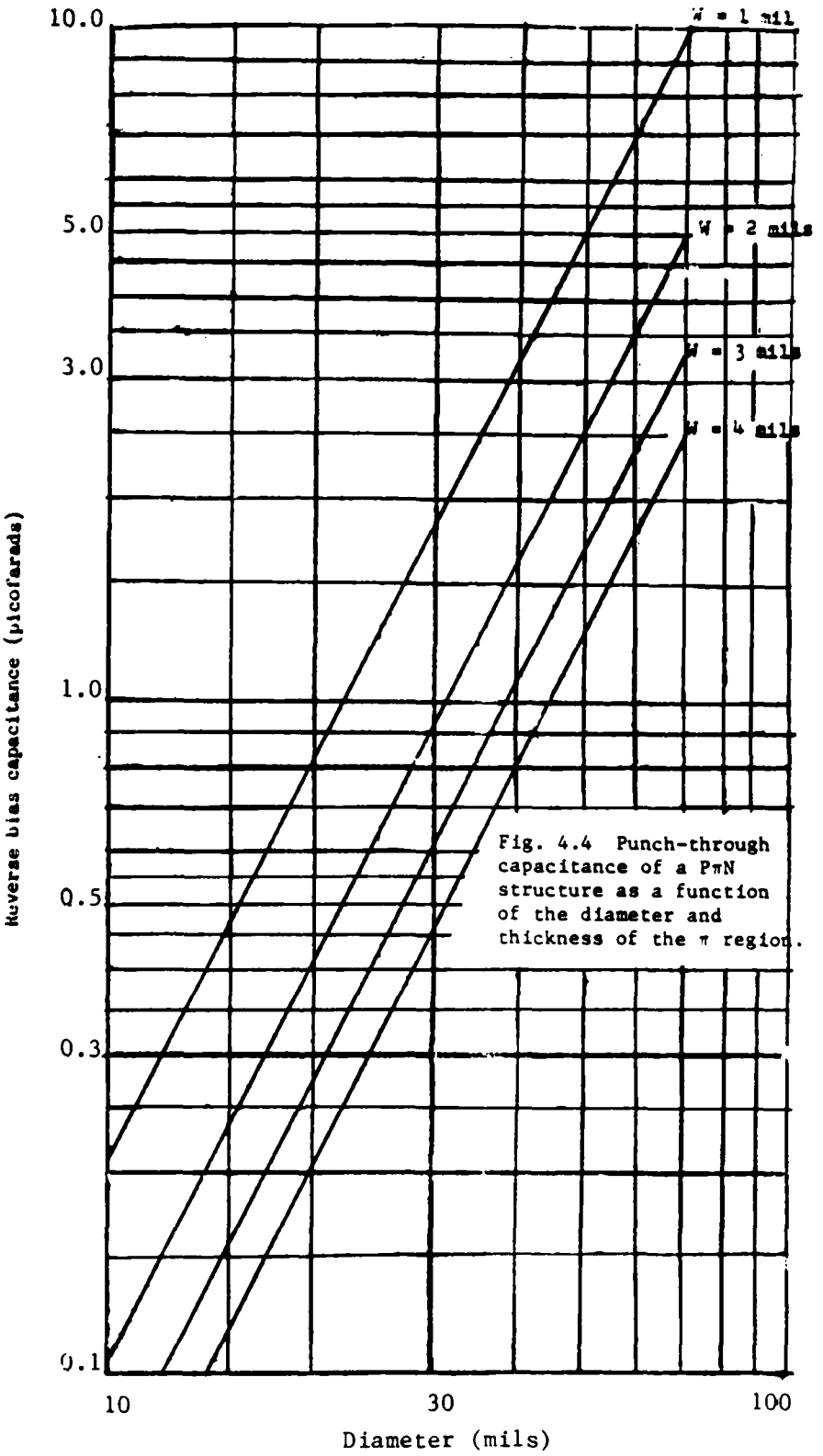



Fig. 4.4 Punch-through capacitance of a PπN structure as a function of the diameter and thickness of the π region.

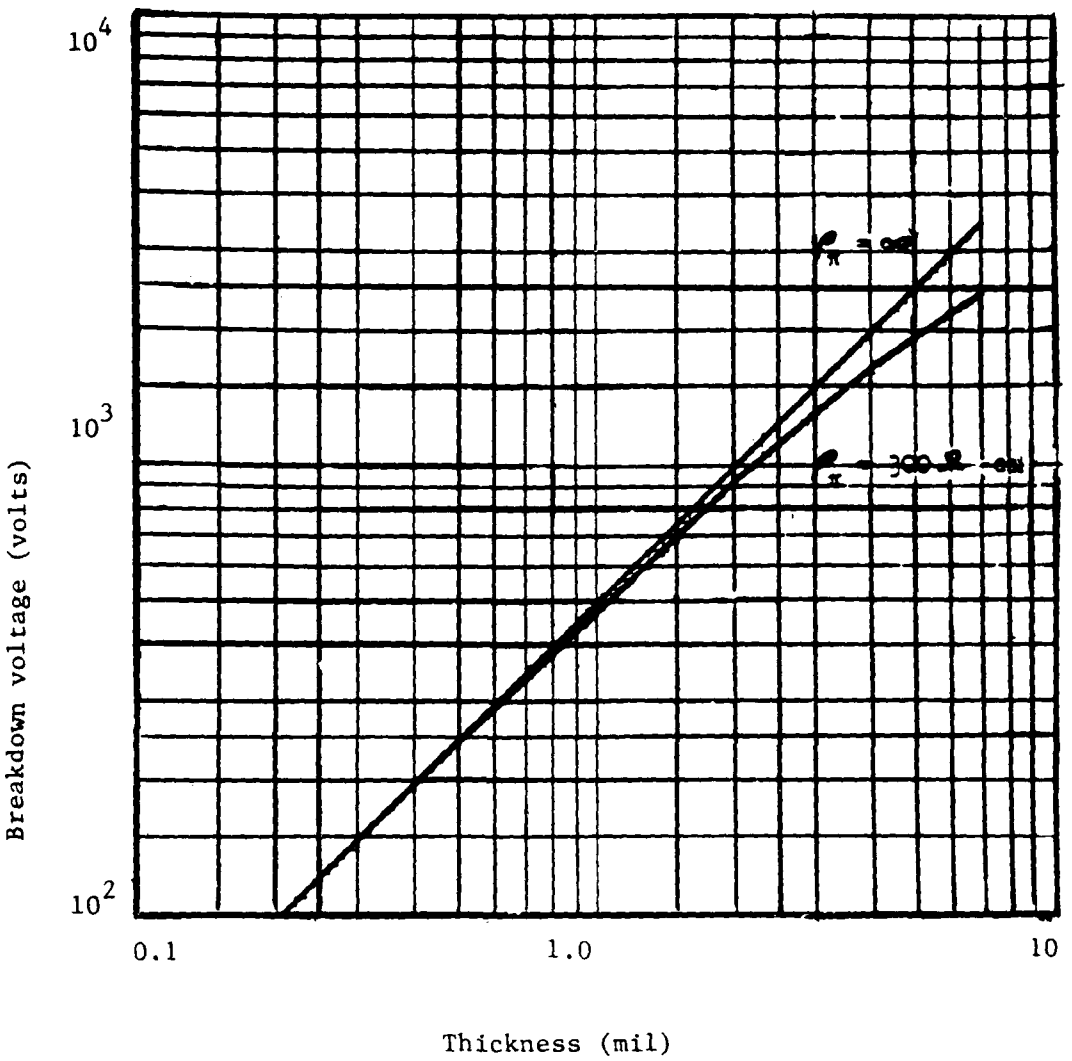



Fig. 4.5 Breakdown voltage of a plane P-N structure as a function of the thickness of the $\pi$ region

planar portion of the junction. The effect of the junction curvature is to increase the maximum electric field at the junction and to decrease the breakdown voltage. An approximate calculation of the reduction of the breakdown voltage, with respect to the breakdown voltage of a planarjunction, is given in Fig. 4.6 in terms of the curvature of the junction and the thickness of the $\pi$-region .

Under forward-bias conditions, electrons from the N region and holes from the P region are injected into the $\pi$ region. The distribution of carriers is shown in Fig. 4.7. The equation which determines the injected carrier distribution is the diffusion equation:

$$D_a \frac{d^2n}{dx^2} - \frac{n}{\tau} = 0 \quad \text{or} \quad \frac{d^2n}{dx^2} - \frac{n}{L^2} = 0 \quad , \qquad (4.7)$$

where $D_a$ is the ambipolar diffusivity and L is the ambipolar diffusion length given by:

$$D_a = \frac{2\, D_e D_h}{D_e + D_h} \quad \text{and} \quad L = \sqrt{D_a \tau} \quad , \qquad (4.8)$$

where $\tau$ is the lifetime of the excess carriers. The spatial distribution of the excess carriers is determined by Eq. (4.7), and from this distribution, the ohmic resistance $r_f$ of the $\pi$ region can be readily determined. It is given by

$$r_f = \frac{2(\frac{kT}{q})}{I_{DC}} \sinh \frac{W}{2L} \left[ \tan^{-1} (\sinh \frac{W}{2L}) \right] \quad , \qquad (4.9)$$

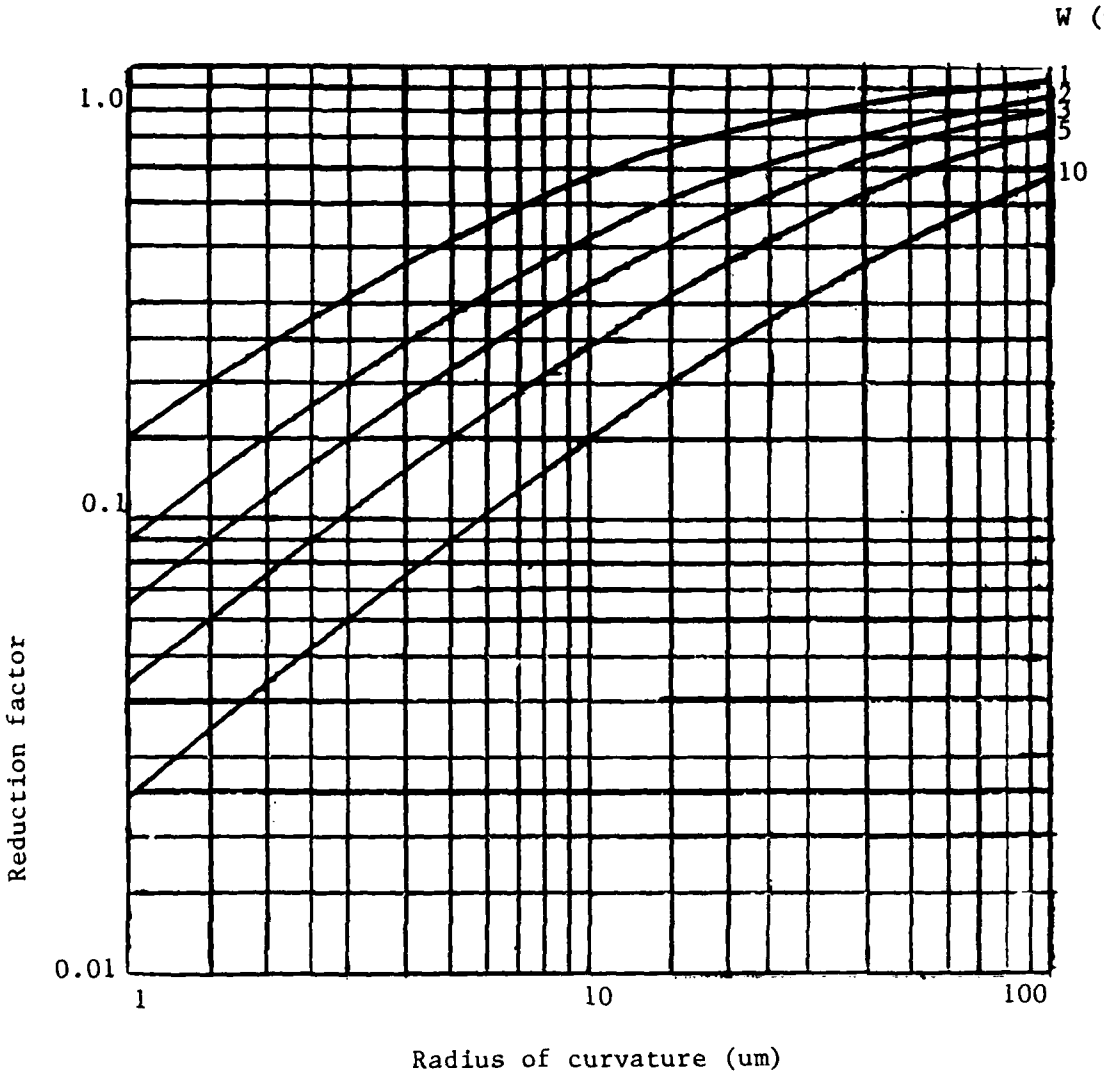



Fig. 4.6 Breakdown voltage reduction factor for a planar PπN structure as a function of the radius of curvature of the diffused regions and the thickness of the π region

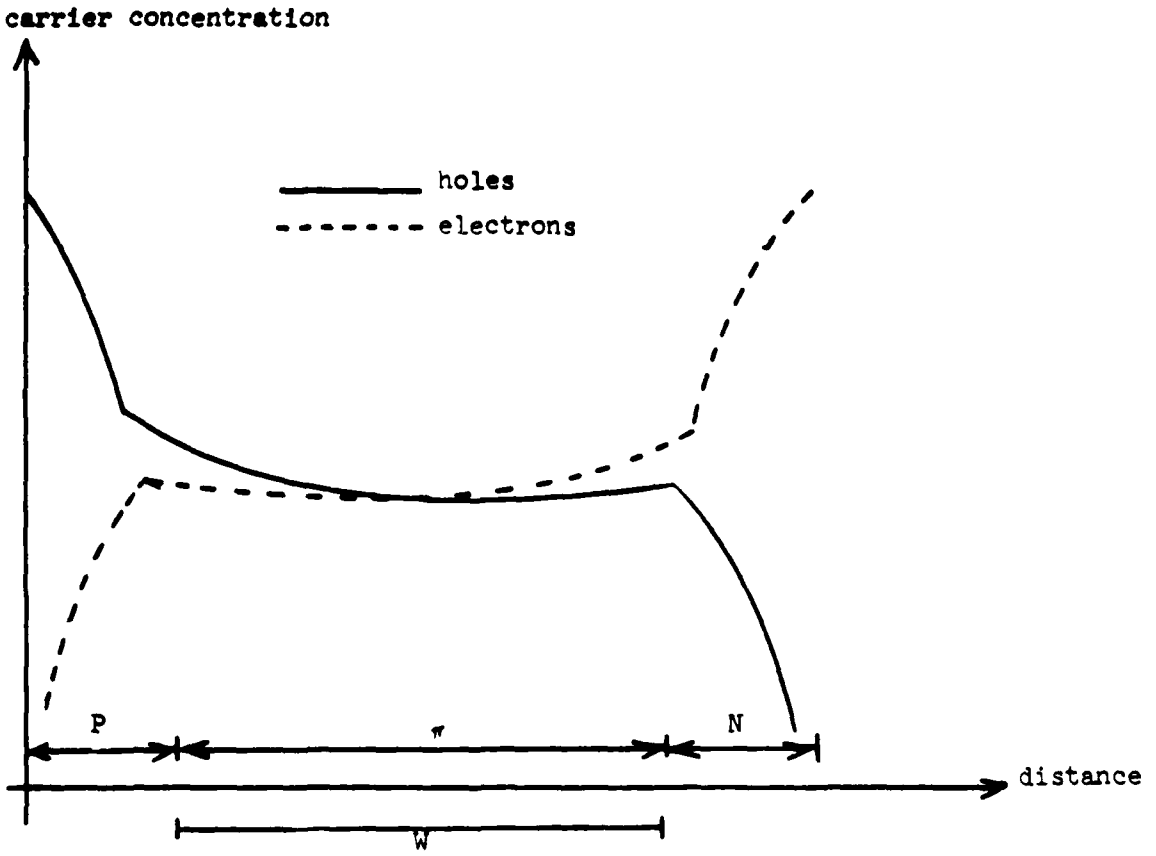



Fig. 4.7 - Schematic representation of the hole and electron distribution in a forward bias PπN diode.

where $I_{DC}$ is the DC bias current, k the Boltzmann constant, q the electronic charge and T the temperature in degrees kelvin. The above equation shows that the product of the forward resistance times the DC bias current is independent of the cross-sectional area and depends only upon the ratio W/2L. Equation (4.9) has been derived upon the assumption of equal mobilities for electrons and holes. When W/2L<<1, that is when the $\pi$-region width is much smaller than the ambipolar diffusion length, Eq. 4.9 reduces to the more conventional form where  is the ambipolar mobility.

$$r_f = \frac{W^2}{2\mu} \quad \frac{1}{I_{DC}\tau} \quad . \tag{4.10}$$

A more accurate calculation of the $r_f I_{DC}$ product, taking into account the difference in hole and electron mobilities in silicon, is given in Fig. 4.8 for T = 300 K. Since the ambipolar diffusion length plays an important role in determining the forward-bias resistance of the P$\pi$N diode, it is plotted in Fig. 4.9 as a function of the carrier lifetime using an ambipolar diffusivity of 18.4 $cm^2$/sec.

The resistance of the P and N regions are independent of the forward current because of the high doping concentration in these regions. The distribution of carriers shown in Fig. 4.7 indicates that the main contribution to total series resistance comes from the resistance of the $\pi$ region, unless the thicknesses of the P and N layers become comparable to the thickness W of the $\pi$ region. Even in the case when the thicknesses of these regions are the same, the injected carrier concentration in the $\pi$ region is two or three orders of magnitude less. Therefore, it is a good approximation to neglect $r_P$ and $r_N$ in the calculation of the total forward resistance.

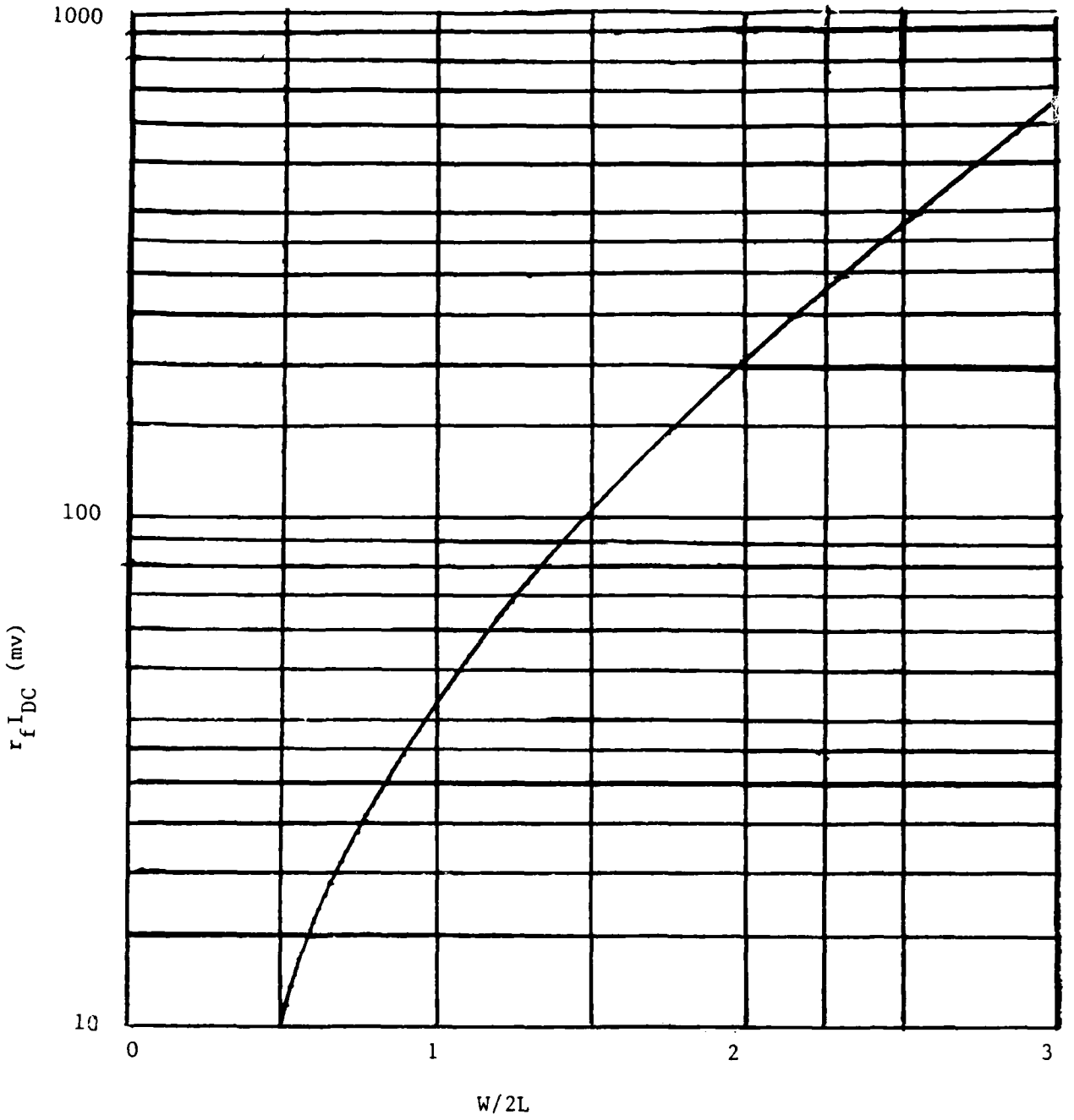



Fig. 4.8 Plot of the $r_f I_{DC}$ product of a PπN structure as a function of W/2L (T - 300°k)

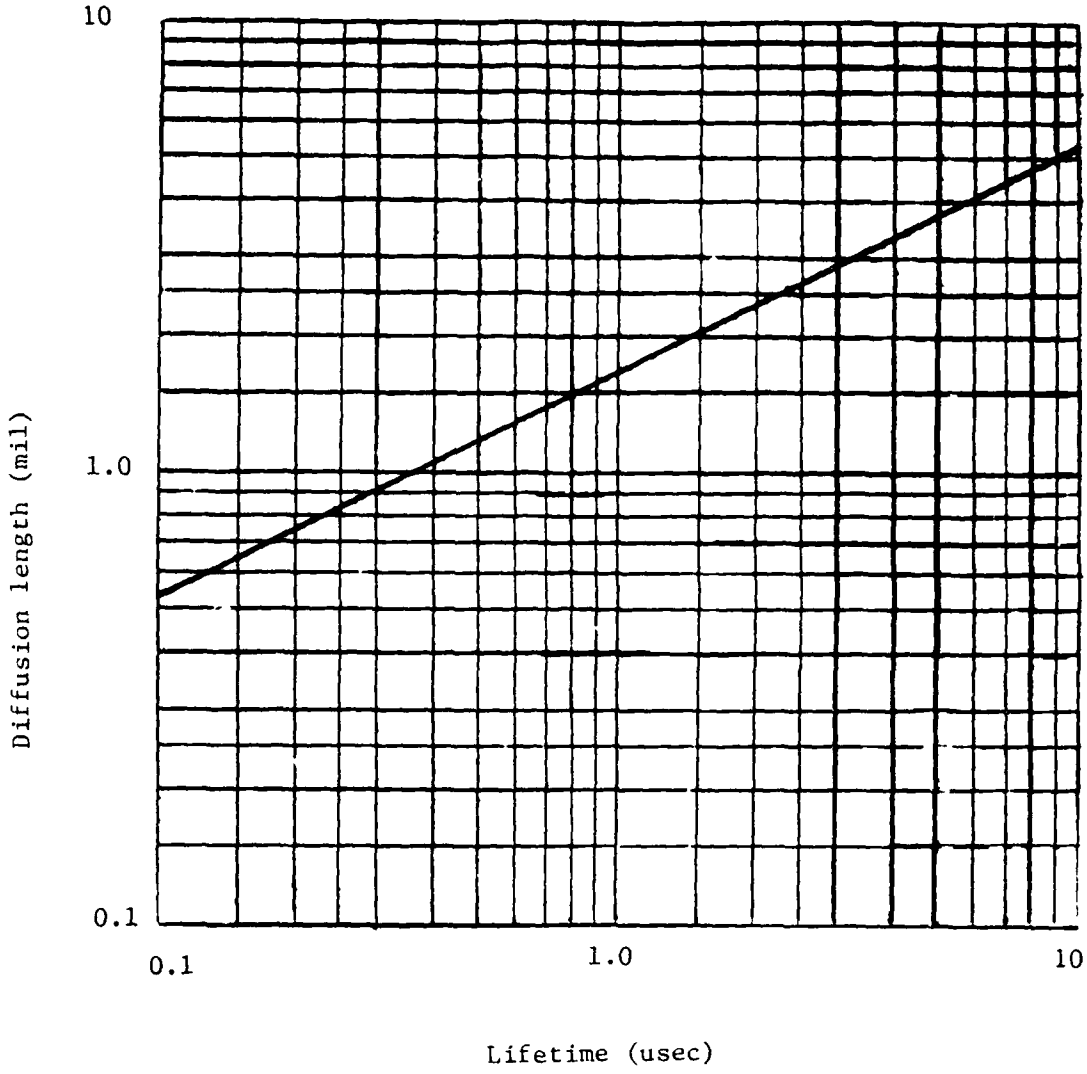



Fig. 4.9 Ambipolar diffusion length as a function of excess carrier lifetime (T = 300°k)

## 4.2 Effect of Recrystallized Silicon-on-Insulator Film on PIN Diode Design

While conventional PIN diode design, as summarized in Section 4.1, is well established, implementation with a silicon-on-insulator technology for MMIC implementation is not straightforward. There are two main concerns:

1. the lifetime of recrystallized silicon films is not well established, raising the basic question whether significant levels of conductivity modulation can be achieved. At a minimum, the ambipolar diffusion length that can be achieved must be investigated in detail.
2. the silicon-on-insulator film combined with MMIC compatibility leads to a very difficult vertical topology. Lateral (surface-oriented) PINs are more compatible with functionally integrated components but neither the on-state conductivity modulation nor the off-state electric field is as uniform. The promising aspect is the inherent high performance of a PIN in a control application. In fact, we believe that the potential of the technology will be eventually limited by a tradeoff between on-state DC bias-current requirements and off-state RF voltage-handling capability, with the key device parameter being the lifetime.

The diode design consists of determining the thickness W of the $\pi$ region, the cross-sectional area A, and the length of the diffused regions.

As an example of the design procedure, let us consider the design of a high-quality, vertical-structure device, diode A, to meet the following requirements:

$$R_f = 2.0 \text{ ohm at } I_{DC} = 100 \text{ ma},$$

$$V_b \geq 400 \text{ volts},$$

$$C_J = 0.25 \text{ pF}.$$

Assuming a parasitic series resistance of 0.2 ohm, $r_f I$ is equal to 180 mV. From Fig. 4.8, a value of 1.90 is obtained for the ratio W/2L. Assuming a lifetime of 1 microsecond, a value of 1.7 mils for L is obtained from Fig. 4.9. Taking into account that at high injection levels L may be half of that value, the value of W is:

$$W = 2 \times 1.90 \times \frac{1.7}{2} = 1.90 \times 1.7 = 3.23 \text{ mils}$$

Fig. 4.5 gives a breakdown voltage of 1400 volts for a planar junction. If the length of the diffused regions is 10 μm, Fig. 4.6 gives a reduction factor of 0.32 in the breakdown voltage, that is, the calculated breakdown voltage is:

$$V_b = 1400 \times 0.32 = 450 \text{ volts}.$$

Considering the uncertainty in the breakdown voltage reduction factor, the thickness of 3.23 mils is acceptable. With the 0.25-pF junction capacitance as a requirement and a thickness of 3.23 mils, Fig. 4.4 gives a diameter of 20 mils, assuming no fringe capacitance. For the planar structure of Fig. 4.1, the diameter of the N dot should be somewhat smaller. A safe factor is to reduce the calculated diameter by an amount equal to the thickness W of the $\pi$ region. In this case, the diameter of the N circular area should be taken as 17 mils.

As another example, let us consider the design of a poorer quality, vertical diode B, more representative of reasonable expectations with recrystallized silicon rather than single crystal, with

$$R_f = 1.0 \text{ ohm at } I = 50 \text{ ma},$$

$$V_b \geq 100 \text{ volts},$$

$$C_J = 0.50 \text{ pF}.$$

Assuming a parasitic resistance of 0.3 ohms, the $r_f I$ product is 35 mv. From Fig. 4.8 a value of 0.90 is obtained for W/2L. Assuming a value of lifetime equal to 0.2 microsecond (or L = 0.75 mils) and taking into account the reduction in the ambipolar diffusion length, we obtain,

$$W = 2 \times 0.90 \times \frac{0.75}{2} = 0.68 \text{ mils (or 17 microns)}$$

The breakdown voltage for a planar junction is 330 volts from Fig. 4.5. Assuming that the depth of the diffused region is 2 μm, the breakdown voltage reduction factor, obtained from Fig. 4.6, is 0.3. That is, the breakdown voltage of the planar junction is:

$$V_b = 330 \times 0.3 = 100 \text{ volts}.$$

This is close to the required voltage. For a $C_J = 0.50$ pF, a diameter of 13 mils is obtained. It should be pointed out that the area cannot be made too small, because the injected carrier concentration in the $\pi$ region is inversely proportional to the area. A very high injected carrier

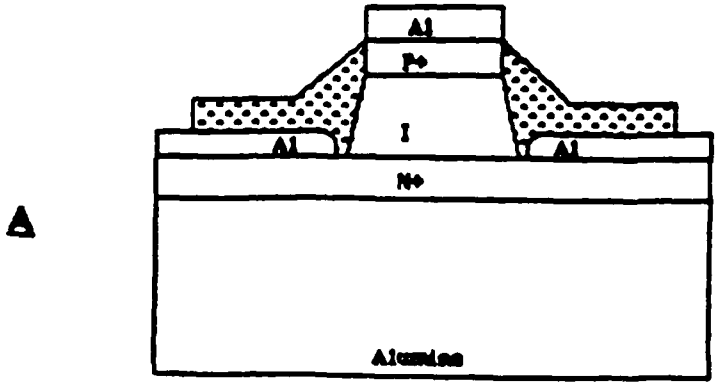
concentration may bring a reduction in the ambipolar diffusion length by a factor larger than the one assumed.

Now if the lifetime is maintained at 0.2 microseconds and we require 2.5 ohms resistance at only 5 mA bias current, assuming 0.3 ohms parasitic resistance and a 1 μm diffusion depth, we obtain a 9.9 micron I-layer width and a breakdown voltage of 60 volts. Thus the tradeoff of on-state bias current (and therefore DC prime power), on-state RF forward resistance and off-state RF power handling is demonstrated.

While the ramifications of a non-uniform lateral design instead of a more-uniform, vertical structure are less obvious, some relaxation of these constraints is indicated. The actual penalty with a lateral surface oriented structure has not been quantitatively determined as yet. However, the effect of recrystallized film quality and processing conditions will be dominant factors.

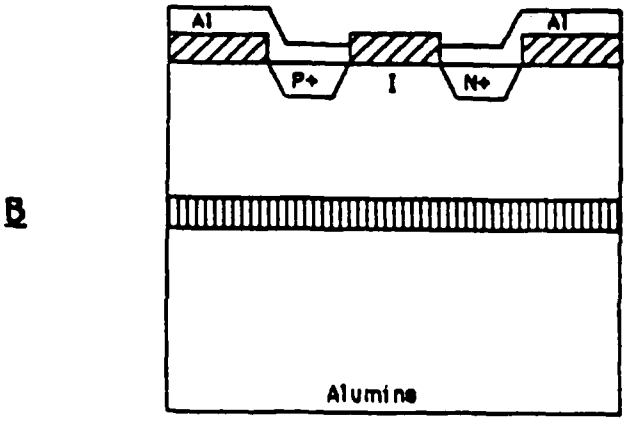
Initially, consider the vertical design of Fig. 4.10A. This conventional PIN structure has a high resistivity epitaxial grown layer over a recrystallized $N^+$ silicon film, followed by conventional silicon processing. Optimization for RF performance (to replace aluminum conductors) is straightforward, but not planned to be included in the programs. The key difficulty is an expected low lifetime region near the $N^+$ recrystallized film and an involved processing procedure to avoid RF spreading resistance loss in the $N^+$ layer (see Appendix B).

While the lateral design of Fig. 4.10B alleviates these conditions to a good degree, we require a purer, higher-resistivity intrinsic layer for lowest dielectric loss than is needed for punch-through at voltages below breakdown (particularly if an I layer thickness approaches 1 mil). More important the non-uniformity of current injection in the on-state and




Note: Drawing not to scale.

Polyimide




Note: Drawing not to scale.

Field Oxide

.5 micron recrystallized poly doped N+

Figure 4.10 Cross-Sectional Views of (A) Vertical and (B) Lateral PIN Diodes

electric field concentration in the off-state leads to an electrical performance penalty as described before.

At this stage we favor the lateral device structure, although mask sets have been designed for both structures as described in Section 4.3.

## 4.3 Mask Designs for Lateral and Vertical Device Structures

Two device designs are under consideration for the realization of a monolithic PIN diode. Fig. 4.10A is the cross-sectional view of the vertical device structure and Fig. 4.10B is the cross-sectional view of the lateral device structure. The recrystallized polysilicon in the vertical device is doped $N^+$, where it serves as the $N^+$ region in the PIN topology. Polyimide is used for the inter-level isolation material between the $N^+$ and $P^+$ metallizations. This inter-level isolation facilitates the monolithic connection of several vertical PIN diodes. The performance-limiting parameter in the vertical structure is spreading resistance in the $N^+$ region. A high value of spreading resistance would cause prohibitive RF losses. The performance-limiting parameter in the lateral topology is the ambipolar recombination lifetime near the surface of the intrinsic region. The forward voltage necessary for significant conductivity modulation in the intrinsic region is a strong function of the ambipolar lifetime. A low value of lifetime results in prohibitively high values of forward voltage to achieve acceptable device performance.

Fig. 4.11 contains a diagram of the masking geometry used for the lateral PIN diode. All dimensions are in microns, and this specific drawing is a PIN diode with a 20-um intrinsic region. The dashed lines correspond to the $N^+$ and $P^+$ implant zones. The lateral mask contains lateral PIN diodes of 6-,10-,20-,30-,40- and 50-um intrinsic regions. The lateral mask

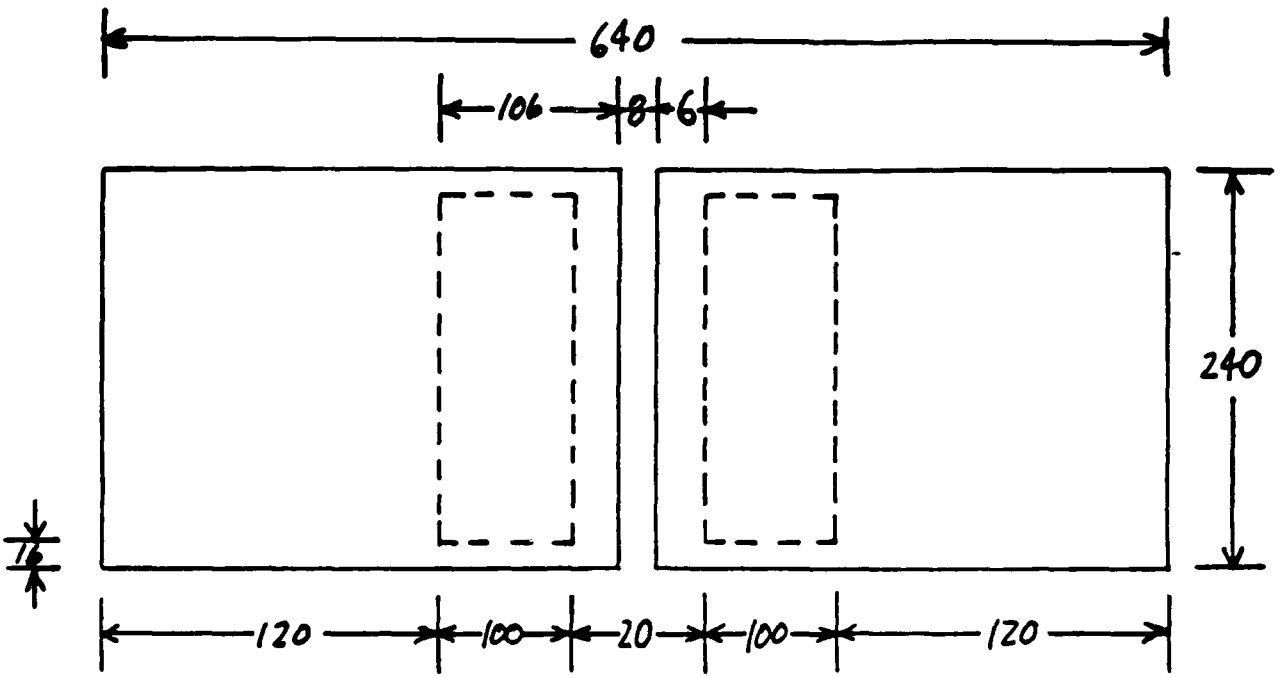
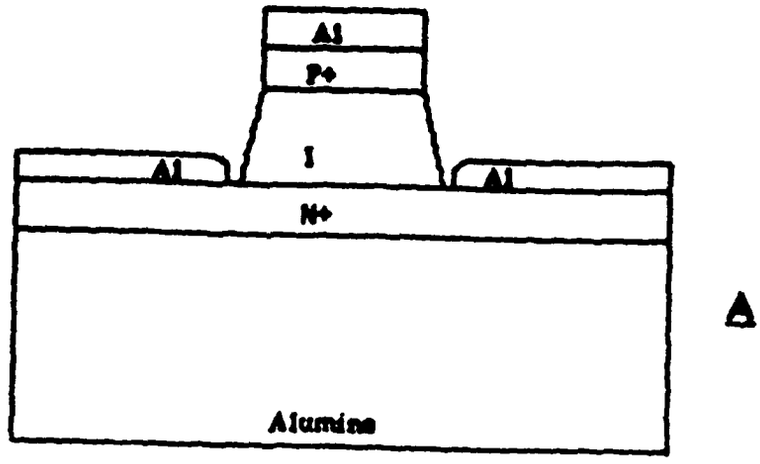



Figure 4.11 Lateral Device Masking Topology
All Dimensions in Microns, Not to scale

also contains a single-pole double-throw switch constructed from 20-um devices. A 6-um and a 10-um device are rotated 90 degrees from the rest of the lateral structures to discern whether the orientation of sub-grain boundaries has a significant influence on device operation.

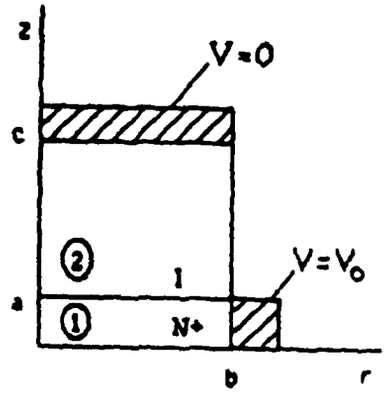
When reviewing Fig. 4.12A, a cross-sectional view of the vertical 'mesa' structure, it becomes evident that the RF spreading resistance of the $N^+$ region could be prohibitively high. Since the skin depth in silicon at the operating frequency is much larger than the thickness of the $N^+$ region, the RF spreading resistance equals the DC spreading resistance.

Fig. 4.12B is the mathematical representation of the vertical device used to obtain an analytic solution of the spreading resistance. An exact solution of the spreading resistance problem entails the solution of Laplace's Equation in cylindrical coordinates subject to the boundary conditions of the vertical structure. Due to the mixed boundary conditions for this problem, classical solution techniques involving orthogonal set manipulations could not be used. However, a unique solution of Laplace's equation was obtained through a novel expansion of the series Bessel Function into coefficient vectors and matrices of infinite dimensions. This linear system represents the potential as a function of distance and conductivity in the vertical structure, and satisfies the conditions of continuous potential and continuous current flow across the boundary of regions 1 and 2. The linear system converges very rapidly, so the coefficient vectors assume finite dimensions. When the coefficient vectors have been obtained, the calculation of the spreading resistance is straightforward. The gradient of the potential is integrated over the respective ohmic contact, which results in $I_{in}$ as a function of applied voltage. The spreading resistance analysis is detailed in Appendix B.




A

Note: Drawing not to scale.




B

Figure 4.12 Cross Section of (A) Vertical PIN Mesa Structure and (B) Model for Spreading Resistance Analysis

## 5. ELECTRICAL CHARACTERIZATION OF THIN SILICON FILMS

It is important to be able to provide electrical characterization of recrystallized silicon films as well as film morphology evaluation. As films with good electrical quality are obtained, PIN diodes will be fabricated using the masks described in Section 4.3 and evaluated at both low frequencies and at microwave frequencies (Section 5.3). However, it is clear from considering PIN diode design that recombination lifetime is a crucial device design parameter which may be difficult to control in recrystallized silicon films. A diagnostic technique which is sensitive to recombination lifetime was considered an important electrical diagnostic of recrystallized film quality.

A related research program underway by one of the principal investigators (R. J. Gutmann with Dr. J. M. Borrego) is exploring microwave-detected photoconductivity-decay as a nondestructive wafer characterization technique (Section 5.1). We have determined a successful implementation technique and have applied it to thin silicon films (Section 5.2).

### 5.1 Microwave-Detected Photoconductivity-Decay for Wafer Lifetime Measurement

In this technique, carriers are generated by irradiating the sample with light of short enough wavelength to produce hole-electron pairs. Since the conductivity of a sample is proportional to the number of carriers, monitoring the conductivity after the light is removed allows determination of the lifetime. Note that the conductivity modulation achieved is similar to forward biasing the PIN diode; however, injecting contacts are not required. While the conductivity of the sample can be monitored by placing ohmic contacts on the material, a more appealing method is to monitor the

conductivity by means of microwave radiation without the necessity of fabricating ohmic contacts. Thus, contacts are not needed for either injection or monitoring purposes.

A simplified treatment of the microwave reflection measurement technique will be presented which focusses on a first-order theory of the relationship between the change in microwave reflection and the density of excess carriers produced by photoinjection. A simplified schematic diagram of the measurement technique is shown in Fig. 5.1. A CW microwave signal source generates a forward wave with power $P_i$ which is directed to the semiconductor sample by the antenna. The semiconductor sample reflects part of this wave whose power is detected by a square law detector through a directional coupler.

The semiconductor wafer is considered to be a lossy dielectric of conductivity $\sigma$, electric permittivity $\varepsilon$ and thickness W. It is assumed that the wafer is backed by a lossless metallic contact which reflects the microwave radiation. In most of the cases measured, the dark conductivity of the semiconductor was small and can be assumed to be zero. In this case, the magnitude of the reflection coefficient $|\Gamma_s|$ of the sample will be unity since all the incident power is reflected.

When the conductivity of the semiconductor is increased to a value $\sigma$ due to photoinjection of carriers, the value of $\Gamma_s$ changes by a small amount $\Delta_s$ due to the increase $P_d$ in power dissipated and we have:

$$|\Gamma_s - \Delta_s|^2 = 1 - \frac{P_d}{P_i} \quad . \tag{5.1}$$

The above equation can be written as:

$$1 - 2r\cos\theta + r^2 = 1 - \frac{P_d}{P_i} \quad , \tag{5.2}$$

where

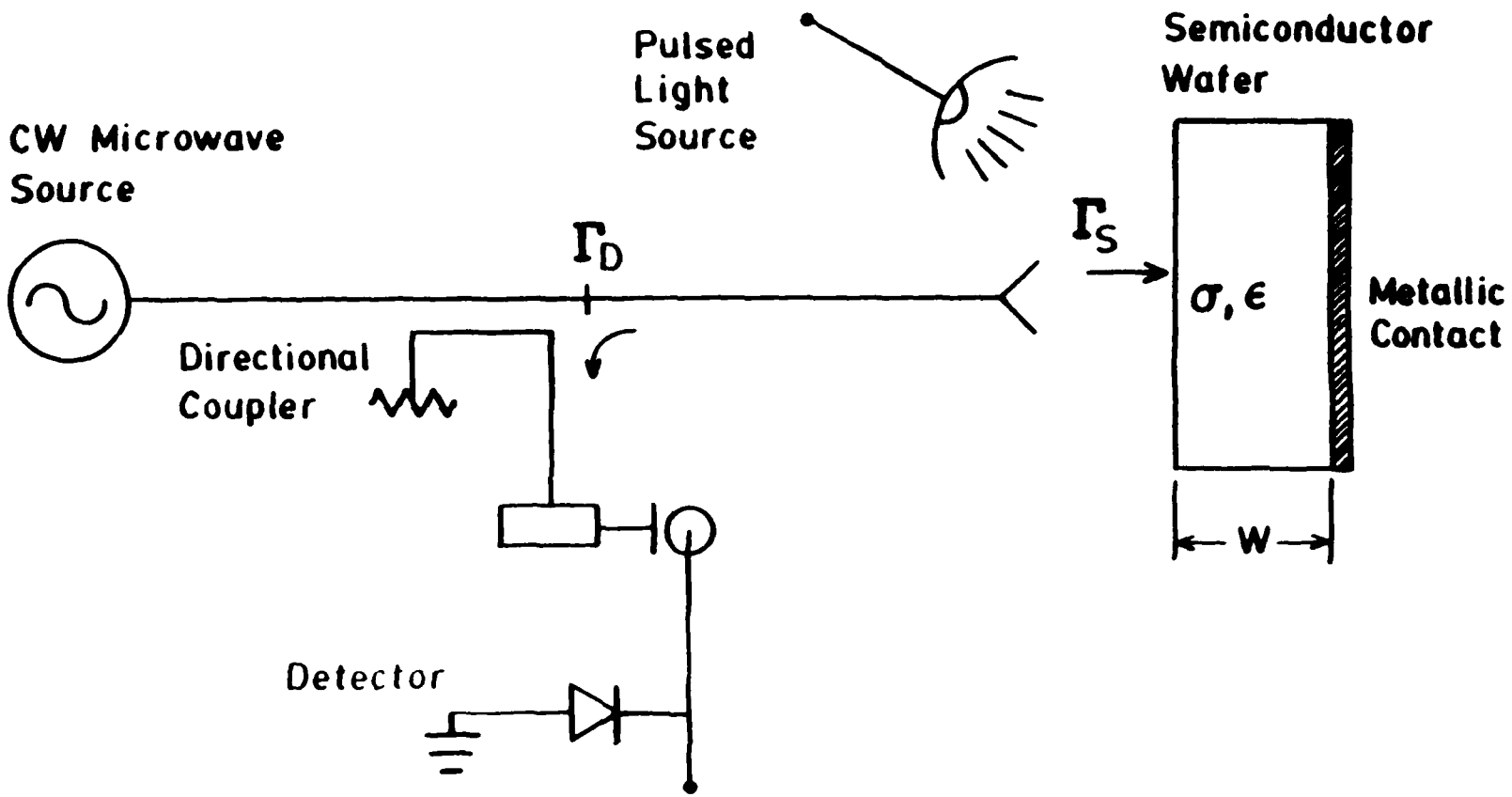



Figure 5.1 Microwave Measurement Concept

$$r = |\Delta \Gamma_s| \quad ,$$

$$\theta = \text{angle of } \Gamma_s^* \Delta \Gamma_s \quad .$$

If $|\cos \theta| << |\Delta \Gamma_s|$ we can approximate Eq. (5.2) by

$$|\Delta \Gamma_s| = \frac{P_d}{2P_i} \quad . \tag{5.3}$$

The dissipated power can be calculated for a given sample thickness. If the sample is thin compared to the wavelength in the semiconductor, then the sample looks like a short and Eq. (5.3) becomes:

$$|\Delta \Gamma_s| = \frac{\pi^2}{6} \left(\frac{4W}{\lambda_o}\right)^2 \sigma W \eta_o \quad , \tag{5.4}$$

where $\lambda_o$ is the free-space wavelength and $\eta_o$ is the free-space characteristic impedance. If the sample thickness is close to a quarter-wavelength then the sample impedance is very high and Eq. (5.3) becomes:

$$|\Delta \Gamma_s| \tilde{\sim} \sigma \eta_o W \quad . \tag{5.5}$$

In both cases, the magnitude of $\Delta \Gamma_s$ is proportional to the sample conductivity $\sigma$ induced by the photoinjection of carriers.

The relationship between the reflection coefficient $\Gamma_s$ at the sample and the reflection coefficient $\Gamma_D$ at the detector is approximated as follows. The microwave system between the detector and the surface of the sample can be considered as a linear reciprocal two-port network described by scattering parameters $S_{11}$, $S_{12}$ and $S_{22}$. The relationship between $\Gamma_D$ and $\Gamma_s$ is given by:

$$\Gamma_D = S_{11} + \frac{S_{12}^2 \Gamma_s}{1 + S_{22} \Gamma_s} \quad . \tag{5.6}$$

By making a Taylor series expansion in the above equation and retaining only the first term we obtain:

$$\Delta \Gamma_D = \frac{S_{12}^2 \Delta \Gamma_s}{(1 + S_{22} \Gamma_s)^2} \tag{5.7}$$

This shows that the change in the reflection coefficient at the detector is proportional to the change in the reflection coefficient at the sample.

In the measuring system that we describe in the next section, the system can be adjusted so that the detector measures the change in the reflection coefficient, i.e., $\Delta \Gamma_D$. Assuming a square-law detector, the voltage output of the detector $V_D$ is proportional to the square of the magnitude of $\Delta \Gamma_D$ so that:

$$V_D \alpha |\Delta \Gamma_D|^2 \alpha |\Delta \Gamma_s|^2 \quad . \tag{5.8}$$

From Eq. (5.4) or (5.5) the magnitude of $\Delta \Gamma_s$ is proportional to the conductivity of the sample:

$$V_D \alpha \sigma^2 \quad . \tag{5.9}$$

The conductivity $\sigma$ is proportional to the excess carriers generated, and it will decay with the same time constant $\tau$ as the carriers decay:

$$\sigma(t) = \sigma(0) \exp - t/\tau \quad . \tag{5.10}$$

Combination of Eqs. (5.9) and (5.10) give:

$$V_D(t) = V_D(0) \exp - 2t/\tau \quad . \tag{5.11}$$

This shows that the detector voltage decays with a time constant $\tau/2$.

The preceeding analysis, although very simplified, helps one to understand the conditions for which the magnitude of the detector voltage can be used for extracting the lifetime of excess carriers.

The microwave measurement set-up used for determining the lifetime of excess carriers by monitoring the decay of the microwave reflection is shown in Fig. 5.2. The microwave part of the system consists of a CW microwave generator which operates in the $K_a$ band range (26 to 40 GHz) and produces an output power of a few milliwatts. The antenna used for directing the CW microwave signal to the semiconductor sample and the crystal detector used for monitoring the reflection of the CW signal are located at two of the

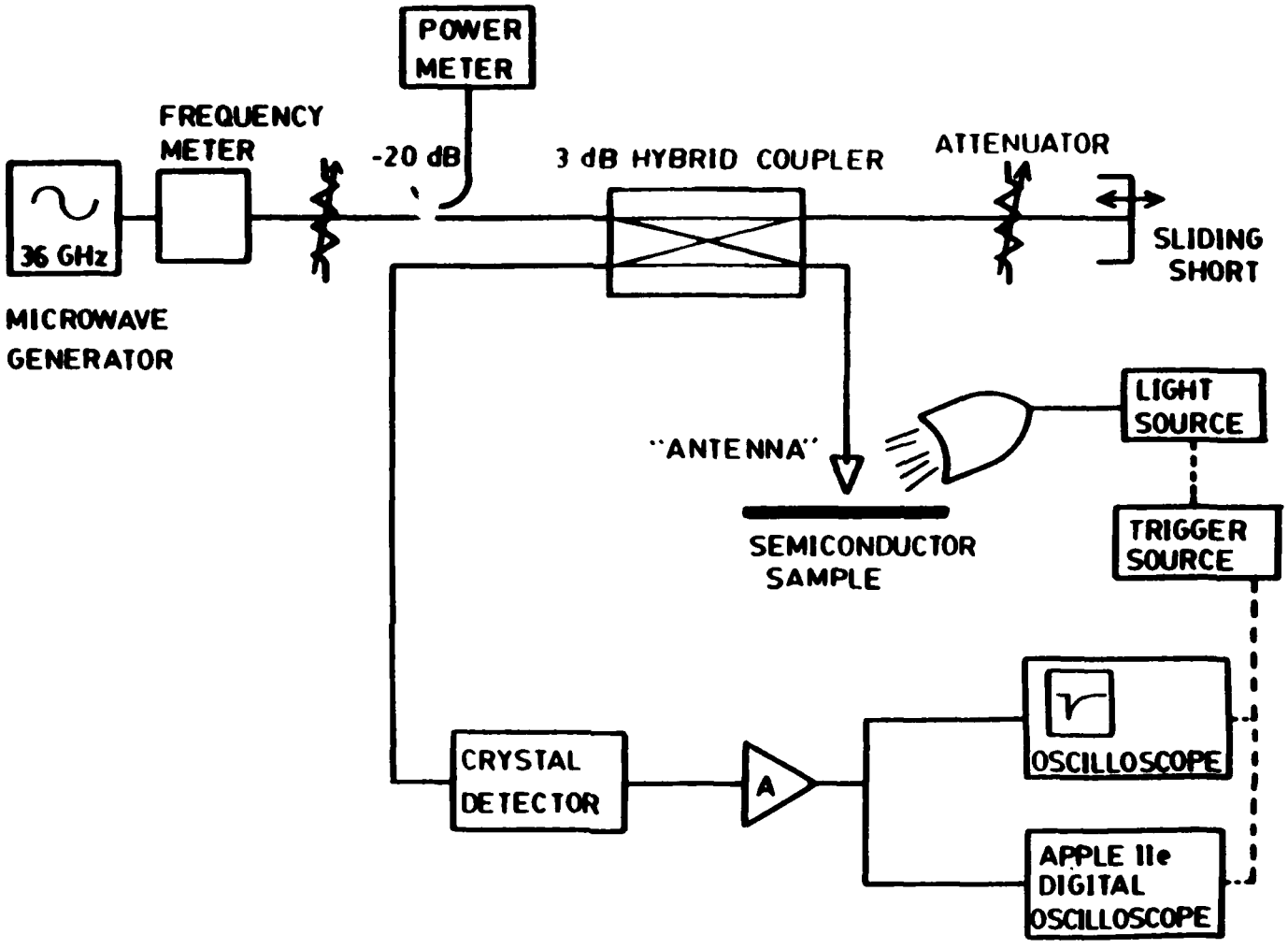



Figure 5.2 Microwave Measurement Setup

four ports of a microwave bridge using a 3-dB hybrid. The other two ports of the bridge have the CW signal as input and an attenuator and a sliding short for maximizing the response of the system to conductivity changes in the semiconductor sample.

The schematic diagram of Fig. 5.2 shows the voltage output of the crystal detector which was monitored with an oscilloscope. An automated data acquisition system uses an Apple IIe computer and a digital memory oscilloscope card to transform the computer into a dual-channel fully programmable digital memory oscilloscope. The digitized waveform was stored on a disk and analyzed in detail. The transient waveform was averaged over a number of cycles in order to reduce the effect of noise in the system.

The other important component of the measuring system is the light source used for injecting the excess carriers in the semiconductor wafer. In this program we used three different light sources whose main characteristics are summarized in Table 5.1. Of the three light sources, the Xenon flashlamp is capable of producing high-level injection in samples doped to $10^{15}$ to $10^{16}$ $cm^{-3}$. In fact, from measurements in silicon solar cells, it is estimated that the lamp produces illumination equivalent to 300 to 500 suns.

Figure 5.3 shows the absorption coefficient of stress-relieved silicon as a function of wavelength. The Xenon lamp produces carriers very close to the surface of the wafer (within the first few μm) while the AlGaAs and GaAs laser sources generate carriers within the first 20 to 40 μm from the wafer surface.

The advantage of using light sources of different wavelength is to probe the lifetime of excess carriers at different distances from the wafer surface. However, this is not a clear-cut procedure since the carriers

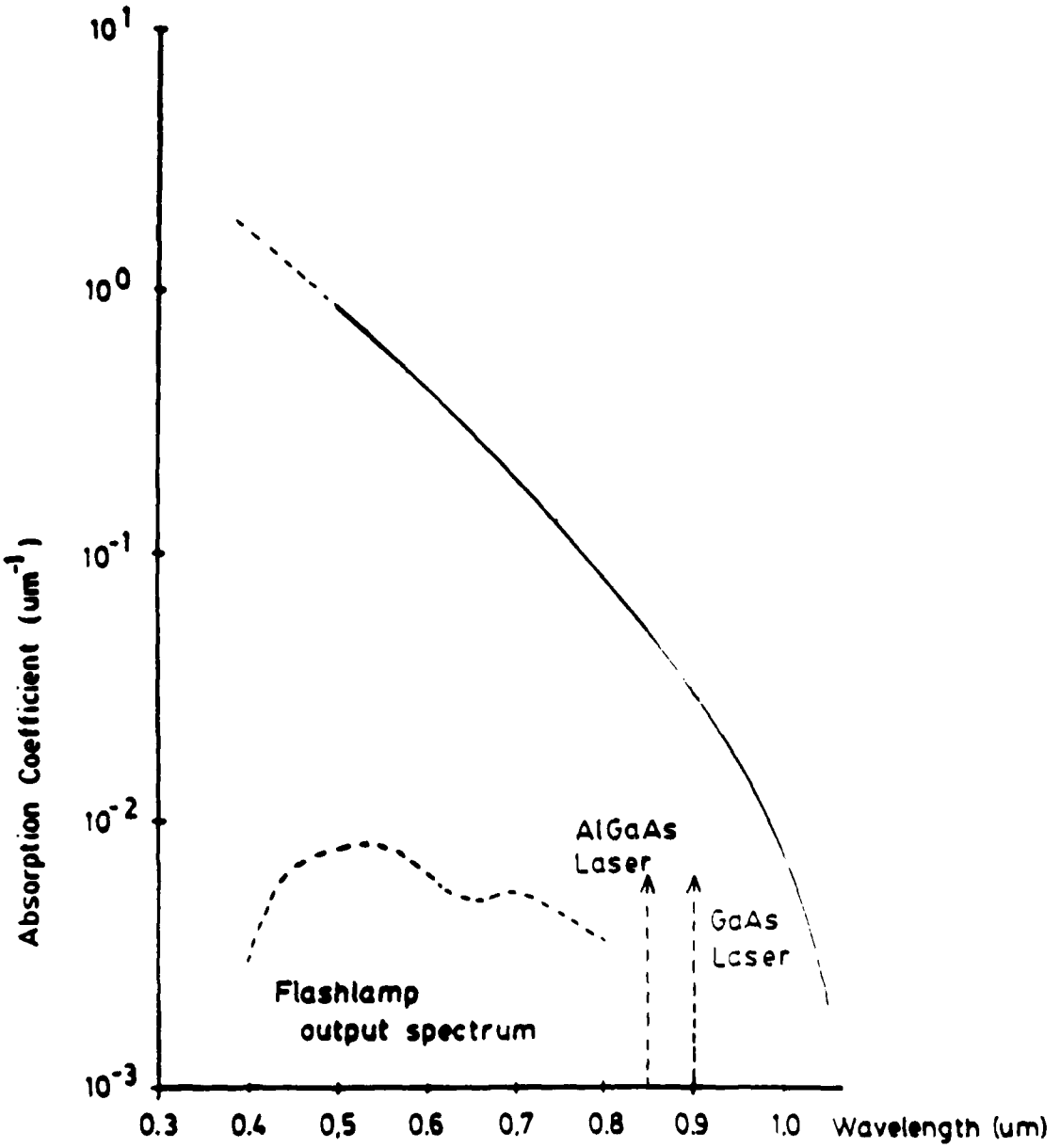



Figure 5.3 Absorption Coefficient of Stress-Relieved Silicon

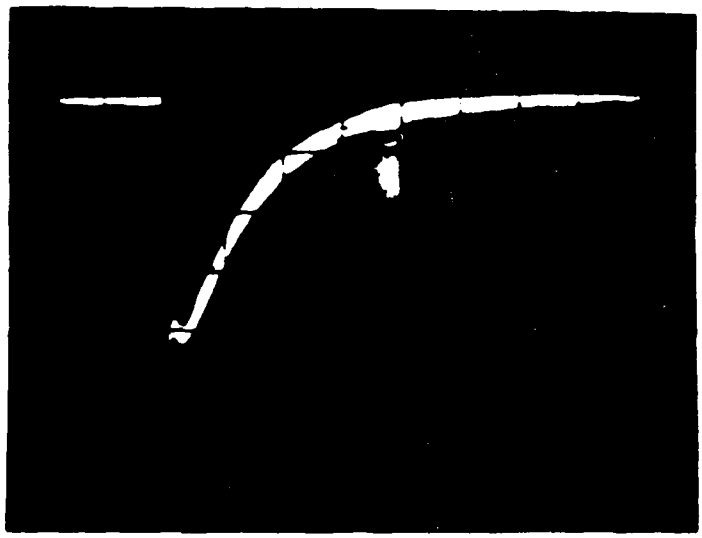
diffuse from the generation point during the optical pulse, thereby reducing the carrier confinement produced by the light source.

The photograph in Fig. 5.4 shows the detector voltage decay as a function of time in a thick oxide-passivated silicon wafer after a pulse of carriers have been injected with the Xenon flash lamp. The time constant $\tau_D$ of the decay which was obtained from the photograph is 278 μs, corresponding to a excess-carrier lifetime $\tau$ of 556 μs according to the first-order theory. Measurement of the generation lifetime of the MOS diodes in the same wafer by the capacitance-transient recovery method gave a generation lifetime $\tau_G$ of 437 μs, surprisingly close agreement. Recent results indicate that the technique can be applied to denuded-zone silicon wafers as well as GaAs wafers, although the interpretation of the transient waveforms is not as straightforward as with uniform, well-surface-passivated silicon.

## 5.2 Application of Microwave-Detected Photoconductivity-Decay Measurement for Thin-Film Evaluation

The sensitivity of the microwave measurement facility is dependent upon the number of electron-hole pairs generated by the optical source and the conductivity modulation achieved. If the film thickness is reduced below the reciprocal of the absorption depth, both the optical absorption and the resultant microwave pulse signal is reduced. With the present microwave system, we do not expect to be able to evaluate recrystallized 0.5-μm-thick films, but we are able to measure 6- to 12-μm thick films after epitaxial growth.

To evaluate the microwave reflectance apparatus on thin films, thinned silicon wafers were obtained from RCA/Lancaster. At RCA, p-type ($10^{15}$ $cm^{-3}$) wafers were thermally passivated via thermal oxidation, then chemically



V. Scale - 50 mV/div

H. Scale - 200 uS/div

$\tau \approx 278$ uS

Figure 5.4 Transient Decay of Well-Passivated Uniform Silicon Wafer.

thinned from the backside to thicknesses ranging from 7 to 15 μm. After processing, the samples had a thermal oxide of 1200-Å thickness on the frontside and an unpassivated backside. The optical generation in the epitaxial layer was accomplished by using the pulsed Xenon and the IR laser diode (Table 5.1). A comparison of the structure of these test films and the desired SOI films for PIN diodes is shown in Figure 5.5.

Recombination lifetime was successfully measured on the thin-film samples using the microwave reflectance apparatus. The measured lifetimes ranged from 0.4 to 2.5 microseconds, the thinner samples resulting in the lowest lifetime values. This phenomenon could be attributed to the unpassivated surface being in closer proximity to the optical generation region, thereby resulting in enhanced surface recombination effects in thinner samples. The lifetime was also measured with microwave and optical incidence from both the $SiO_2$ surface to discern whether the thermal oxide has any bearing on the measured lifetimes. Enhanced absorbtion of the optical excitation was observed with frontside incidence, as the 1200-Å thermal oxide is close to an ideal quarter-wave impedance transformer at optical frequencies. A slight trend toward longer lifetimes at incidence through the silicon was observed, as depicted in Table 5.2.

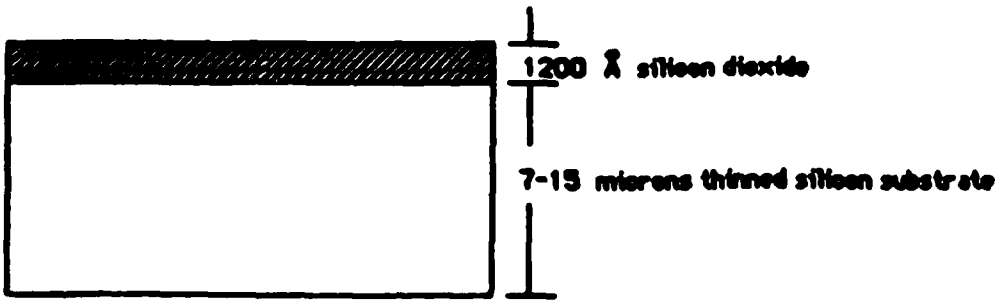
In summary, the microwave reflectance apparatus provides a technique for measuring recombination lifetime in the epitaxial intrinsic layer of a PIN diode. The viability of this technique for the current program depends upon the lifetime and film thickness. The potential for evaluation of recrystallized 0.5-μm films prior to epi growth does not appear feasible at this time. We expect to be particularly sensitive to the epi/recrystallized Si/alumina interfaces if these interfaces are not appropriately passivated.

Table 5.1

Light Sources Characteristics

| Source | Power out | Pulse duration | Wavelength (nm) |
|---|---|---|---|
| Xenon Flash | 30 $W/cm^2$ | 3 μs | ≈ 550 |
| Light Generator (AlGaAs Laser) | 3 mW | Variable up to CW | 850 |
| GaAs Laser | 10 W | 150 ns | 904 |

A




B

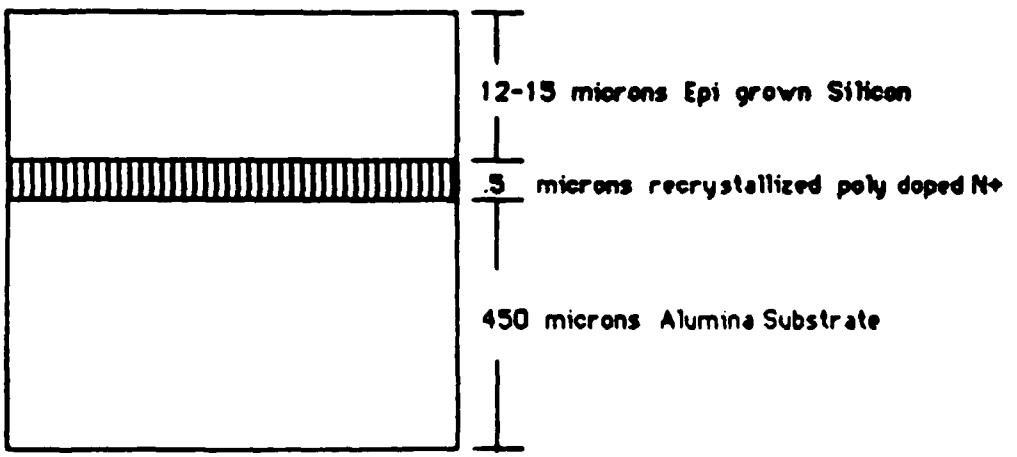



Figure 5.5

A. films evaluated

B. films desired for SOI PIN diodes

Table 5.2

Photoconductivity-Decay Transient Measurements

Thin Films

| Silicon Wafer Approximate Thickness (μm) | | Decay Time (μs) $SiO_2$ Incidence | Decay Time (μs) Si Incidence |
|---|---|---|---|
| 9 | Flashlamp | 2.0 | 2.0 |
| | IR laser | 0.4 | 0.4 |
| 12 | Flashlamp | 1.7 | 2.5 |
| | IR laser | 0.9 | 1.5 |

## 5.3 Conventional Low Frequency and Microwave Data

As recrystallized films with epitaxial layers are obtained with sufficient electrical quality, complete PIN diodes will be fabricated and electrically evaluated. While the detailed structure of these devices can not be determined at this time, basic electrical testing will be similar for any fabricated diodes.

Static I-V characteristics will be obtained with a conventional curve tracer (and picoammeter) to verify junction leakage current and forward-current n factor ($I \propto e^{qV/nkT}$). It is particularly crucial to demonstrate PIN behavior and significant conductivity modulation. Breakdown voltage will be used as an indicator of junction uniformity.

Diode junction capacitance will be measured as a function of reverse voltage to obtain the punch-through voltage and to indicate I-layer doping concentration and thickness. These results are easier to obtain with large-area junctions, but the lateral device may require a three-terminal measurement to obtain the parameters with reasonable precision.

Microwave measurements of unpackaged diodes will be measured at 2-3 GHz under both forward and reverse bias. Particular attention will be placed upon obtaining good small-signal equivalent circuits. An evaluation of $R_f$ versus DC bias current is an excellent test of PIN diode quality (i.e., lifetime), and will be the dominant RF test of recrystallized Si film quality.

# 6. Plans for Second Year

In this section we describe our research plans for the second contract year. As in the first contract year, we are dividing the work into two

major efforts. The first concerns silicon-on-alumina recrystallization problems and sample preparation (Section 6.1). The second concerns the general problem of PIN diode fabrication on silicon-on-insulator films (Section 6.2).

## 6.1 Recrystallization Experiments and Characterization

Two problems related to silicon-on-alumina sample preparation need to be resolved. The first concerns the degree of surface irregularity (+/- 0.1 μm minimum) which is inherent to the starting alumina substrates. We hope to alleviate this problem by one of several procedures (in order of desirability):

- o deposition of a phosphorus-rich glass and reflow prior to silicon deposition.
- o utilization of thicker silicon films.
- o development of a chemical- or plasma-etch planarization process.

Once a procedure has been established for depositing silicon films which are reasonably smooth, we shall have the encapsulation films prepared at another laboratory by means of a process which is known to work reliably for the case of silicon films over oxidized silicon substrates. We hope to eventually obtain an encapsulation layer deposition process for our own laboratory, but we believe that this is not of central importance to our program at this time. After sample preparation problems have been resolved, we intend to perform a variety of recrystallization experiments using the electron-beam system. Similar experiments will be performed with a graphite-strip-heater apparatus as controls. Samples which have good crystallographic texture and low defect densities will be used for PIN diode fabrication.

## 6.2 PIN Diode Fabrication and Characterization

After considering the advantages and disadvantages of the vertical and lateral structure, we have decided to emphasize the lateral structure during the next year, principally because of the compatibility with monolithic circuit fabrication, elimination of the large RF spreading resistance and potential separation of recrystallization defects and the active region of the device.

During the next quarter the lateral device mask set will be finalized, including mostly discrete PINs but also a SPDT switch and test structures. While emphasizing recrystallization experiments, PIN diode aspects unique to the lateral structure will be investigated while the mask set is obtained externally.

After the mask set is received, PINs will be fabricated:

1. starting with high resistivity silicon wafers to debug our processing procedures and to permit the lateral geometry effects to be quantified.
2. starting with silicon recrystallized over $SiO_2$ (then layer over a $S_i$ wafer) to obtain a baseline capability for conventionally recrystallized silicon.
3. starting with silicon recrystallized over alumina (after appropriate planarization as described in Section 6.1).

While the third series of PIN diodes is of direct interest in our research, we believe that the first two steps are necessary to provide an appropriate data base for evaluation of the potential of the SOI technology for monolithic PIN diode phase shifters.

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## Appendix A

### PIN Diode Overview

A PIN diode is a PN junction device with a doping profile such that an intrinsic layer, the I region , is sandwiched in between a P layer and an N layer, as shown in Fig. A.1. In practice, the idealized I region is approximated by either a high resistivity P layer (referred to as $\pi$ layer) or a high resistivity N layer (referred to as $\nu$ layer). The doping profile of a diffused P$\pi$N structure is shown in Fig. A.2. Without any bias, a depletion layer is formed at the junction of the N and $\pi$ layers as shown in Fig. A.3. The extent of this depletion layer is a function of the resistivity of the $\pi$ layer, and for a $\pi$ layer resistivity of 300 ohm-cm, the depletion layer width is of the order of 4 microns.

With a reverse bias voltage applied to the diode, mobile carriers are removed from the $\pi$ layer and the depletion layer penetrates further into the $\pi$ region. If sufficient reverse voltage is applied to the diode, all the mobile carriers are removed from the $\pi$ layer, referred to as the punch-through condition. Any further increase in voltage will not increase the thickness of the depletion layer by any appreciable amount, although the electric field in the $\pi$ region always increases with applied reverse voltage. When the electric field in the depletion layer is high enough, avalanche breakdown occurs. Depending upon the thickness and resistivity of the $\pi$ region, either punch-through or avalanche breakdown occurs at a lower voltage.

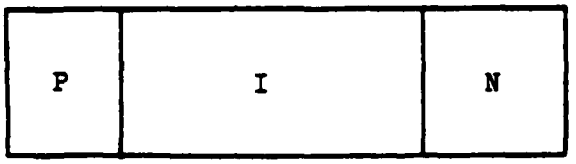



Fig. A.1 Structure of a PIN diode

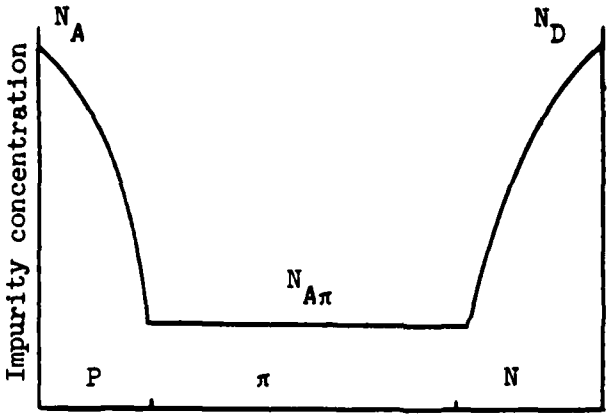



Fig. A.2 Doping profile of a diffused PπN diode

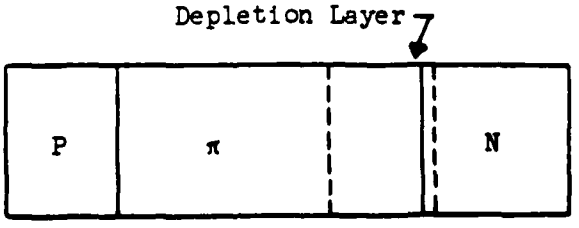



Fig. A.3 Depletion layer in a PπN diode

With a forward voltage applied across the diode, the P region positive with respect to the N region, holes from the P region and electrons from the N region are injected into the $\pi$ region. The injected carriers create a quasi-neutral plasma which increases the conductivity of the $\pi$ region. Another effect of the applied voltage is to decrease the width of the depletion layer between the $\pi$ and N regions. The number of carriers injected into the $\pi$ rgion depends upon the forward current, upon the thickness of the $\pi$ region and upon the lifetime of the injected carriers. If the doping of the P and N regions is high enough, applied reverse and forward voltages do not change the electrical conductivity or the thickness of these regions.

The previous discussion has shown that four regions can be distinguished in a P$\pi$N diode. Two of these regions are the highly doped P and N regions whose characteristics are independent of the bias applied. The other two regions are the depletion layer formed at the junction of the N and $\pi$ regions and the $\pi$ region itself. Therefore, the equivalent circuit of the P$\pi$N diode is as shown in Fig. A.4. The resistances $r_P$ and $r_N$ represent, respectively, the ohmic resistance of the P and N regions, which include the regions of graded doping. As already mentioned, these resistances are independent of bias and their value may change with frequency because of the skin effect.

In the punch-through condition, which is a desirable mode of operation, the undepleted $\pi$ region is absent and the conductance $G_d$ of the depletion layer is small. Therefore, the equivalent circuit reduces to the one shown in Fig. A.5, which can also be represented as a parallel combination of a capacitance $C'_d$ and a resistance $R_r$. If the Q of the diode is high enough, $C_d$ and $C'_d$ are approximately the same.

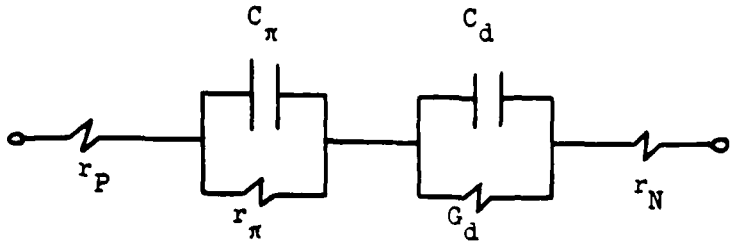



Fig. A.4 Equivalent circuit of a PπN diode

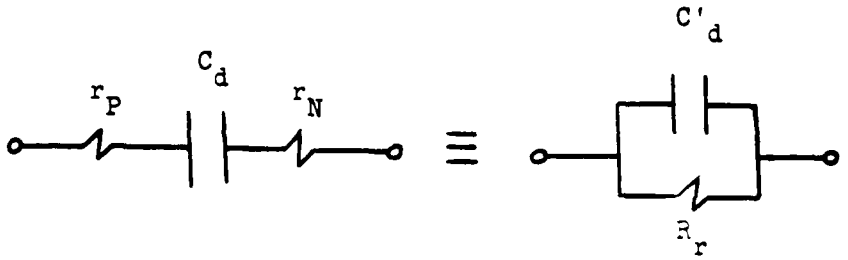



Fig. A.5 Equivalent circuit of a PπN diode under punch-through conditions

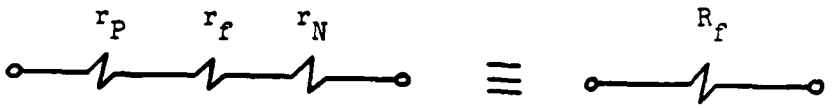



Fig. A.6 Equivalent circuit of a PπN diode at forward bias

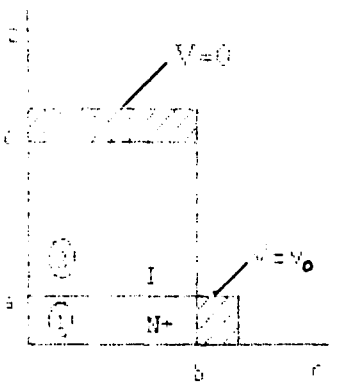
Under forward bias conditions, the capacitance and conductance of the depletion layer become very large and can be neglected. Furthermore, since the resistance of the $\pi$ region is decreased by carrier injection, the capacitance $C_\pi$ can also be neglected. The resulting equivalent circuit is as shown in Fig. A.6. The three resistances can be lumped in a single resistance $R_f$. The contribution of $r_P$ and $r_N$ to the total series resistance $R_f$ depend upon the thickness of the P and N regions and the thickness and injection level into the $\pi$ region. In thin P$\pi$N diodes, $r_P$ and $r_N$ make the same contribution to $R_f$ as $r_f$, while in thick P$\pi$N diodes, $r_f$ is almost equal to $R_f$.

The key aspects of a PIN diode for microwave control applications are the following:

- o high resistivity I layer for punch-through at low DC bias voltage (for low off-state loss)
- o high lifetime so that appreciable conductivity modulation can be achieved (for low on-state loss)
- o low parasitic resistances and capacitances so that inherent device capabilities are not degraded
- o uniform device structure so that on-state injection is uniform and off-state premature avalanche does not occur.

# APPENDIX B
## Analytic Solution Technique

While evaluating the relative merits of the lateral and vertical PIN structures, it is apparent that the RF spreading resistance of the vertical structure could be significant. A large value of spreading resistance results in large resisitive parasitics for the structure and degrades the switching performance of the control device. The RF spreading resistance reduces to the DC spreading resistance as the skin depth at the operating frequency is much greater than the film thicknesses. To obtain an analytic solution for the spreading resistance, one must solve Laplace's equation in cylindrical coordinates for the N+ and the intrinsic region of the vertical PIN. The two dimensional model below is an aproximate model for the vertical structure, with cylindrical symmetry about the z axis. The shaded regions represent ohmic contacts at reference potentials. The boundary conditions of the specified problem are mixed, which invalidates the classical solution technique of the Bessel-Fourier type expansion. However, a specific solution for the spreading resistance may be obtained by expanding the general solution into an infinite linear system. This solution approach is outlined below.




BOUNDARY CONDITIONS

Region #1 ($N^+$)

$$\left.\frac{\partial V_1(r,z)}{\partial z}\right|_{r=0} = 0$$

$$\left.\frac{\partial V_1(r,z)}{\partial z}\right|_{z=0} = 0$$

Region #2 (I)

$$\left.\frac{\partial V_2(r,z)}{\partial r}\right|_{r=0} = 0$$

$$\left.\frac{\partial V_2(r,z)}{\partial r}\right|_{r=b} = 0$$

$$V_1(r,z)\Big|_{\substack{r=b \\ z\le a}} = V_0 \qquad V_2(r,z)\Big|_{z=c} = 0$$

INTERFACE BOUNDARY CONDITIONS

$$V_2(r,a) = V_1(r,a)$$

$$\sigma_1 \nabla_z V_1(r,a) = \sigma_2 \nabla_z V_2(r,a)$$

The general form of the solution can be shown to be:

$$V(r,z) = \Sigma [\, A_n \cosh(kz) + B_n \sinh(kz) \,] J_0(kr)$$

where k is a separation constant.

Through application of the mixed boundary conditions to the boundary value problem, it can be shown that

$$V_1(r,z) = V_0 + \Sigma A_n J_0(m_{on} r/b) \cosh(m_{on} z/b)$$

$$V_2(r,z) = \Sigma B_n J_0(m_{1n} r/b) \sinh[m_{1n}/b(z - b)]$$

where $m_{on}$ = zeros of the Zeroth Order Bessel Function
$m_{1n}$ = zeros of the First Order Bessel Function

When applying the interface boundary conditions, it is evident that the classical orthogonal expansion techniques do not apply. Specifically,

$$\int_0^{\infty} x J_0(m_{on} rx/b) J_0(m_{1n} rx/b) \partial x \neq 0$$

which invalidates the Bessel-Fourier type expansion solution technique. To alleviate this problem, the integrand of the above integral was expanded into a Gamma Function series and integrated. Both interface boundary conditions were expressed as an infinite linear system.

Specifically, the interface boundary conditions of continuous potential and continuous current flow between regions 1 and 2

$$V_1(r,a) = V_2(r,a)$$

$$\sigma_1 \frac{\partial V_1(r,a)}{\partial z} = \sigma_2 \frac{\partial V_2(r,a)}{\partial z}$$

where applied to the potential equations

$$V_1(r,z) = V_0 + \Sigma A_n J_0(m_{on} r/b)\cosh(m_{on} z/b)$$

$$V_2(r,z) = \Sigma B_n J_0(m_{1n} r/b)\sinh[m_{1n}/b(z - b)]$$

The two resulting integral equations obeying the interface boundary conditions were transformed into a linear system using a Gamma Series expansion of the Bessel Function and an integration was performed.

Hense,

$$V_1(r,a) = V_2(r,a)$$

$$\sigma_1 \frac{\partial V_1(r,a)}{\partial z} = \sigma_2 \frac{\partial V_2(r,a)}{\partial z}$$

become

$$\mathbf{FI + GA = HB}$$

and $$\mathbf{MA = NB}$$

where **A** and **B** are coeficient vectors of $A_n$ and $B_n$. This linear system which consists of vectors and matrices of infinite dimensions converges very rapidly in n, and can be solved explicitly for $A_n$ and $B_n$.

When the coefficient vectors have been attained, the solution for the spreading resistance is straightforward. To attain the spreading resistance, integrate the gradient of $V_1$ over the ohmic contact at r=b.

$$I_{in} = 2\pi r_0 \int_0^a \sigma_1 [\partial V_1(b,z)/\partial r]\, dz$$

The exact solution of this integral is very difficult because of the complexity of the gradient term. A zeroth order solution has been obtained which indicates that the spreading resistance of the vetical PIN would indeed be prohibitively high ( 10 Ω ). During the second year of the program, an exact solution of the spreading resistance as a function of the conductivities of the intrinsic region and the N+ region will be obtained. Since the solution will be a function of the conductivities of regions 1 and 2, the spreading resistance may be evaluated for a wide range of injection levels and cylindrical geometries.

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